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Research Article

Stable Delay of Microstrip Line with Side Grounded Conductors

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Characteristics of transmission lines are addressed. Wave impedance and per-unit-length delay of the microstrip structure with grounded side conductors on three layers are calculated under different parameters of the structure. A line which provides the desired value of wave impedance and constant per-unit-length delay, at the expense of correction of the gaps on different layers, is proposed.

Immense growth of wireless communications is ensured by high-performance equipment. There are various requirements for different characteristics of the equipment; for example, some characteristics shall be as high or low as possible, defined in the wide range, or stable with variations of parameters. Often it is necessary to satisfy such requirements simultaneously, which is difficult and expensive. Unfortunately, uncertainty due to the manufacturing tolerance makes additional contribution to the problem. Therefore, simple and cheap solutions permitting to achieve the desired characteristics are required. Features of wireless communications equipment impose wide usage of printed circuit board (PCB) transmission lines, for which the above considerations are in force. For a long time, a number of papers (see, e.g., [1, 2]) have been revealing options providing stable characteristics of single and coupled double-layered dielectric PCB transmission lines obtained only by proper choice of parameters. However, wide usage of multilayered PCBs, higher frequencies, and phase modulation in wireless communications equipment requires seeking new solutions, particularly regarding the stable delay of a transmission line.

For an effective solution it is important to use, as much as possible, resources already existing in a structure to be improved. For the considered case, resources of a multilayered PCB structure, particularly the existence of several dielectric layers, the metallization of these layers, and the possibility to change locally the metallization, can be utilized. Thus, due to domination of multilayered PCBs the proposed approach seems quite general. Let us consider one particular case being very widely used in practice.

During PCB design it is often required to provide a given value of microstrip line characteristic impedance (Z). In those cases, when dielectric placed under the strip is thin, width can be small and therefore its tolerance can influence the value of Z. To increase the strip width, the cuts in ground layers are made under the strip, which increases total dielectric thickness (Figure 1). However, the side conductors affect the value of Z. In addition, they will influence per-unit-length delay (τ) of a line. Preliminary results of this influence have been published [3], and possibility of its useful application has been revealed and recently patented [4]. Unfortunately, it is not a wide circle of specialists who are aware of this information that is important for a design of real PCBs.

The purpose of this work is to show this influence and a possibility of its usage in one paper available to wide audience of the R&D communities working in academia and the telecommunications and networking industries. To achieve this goal, we should estimate characteristics of a microstrip line with the different number of side grounded conductors on different layers. Measurements of a prototype are useful for this purpose. However, it can be expensive as a number of designed and manufactured prototypes can be necessary. Therefore, it is used for a final prototype at final design stage, while for preliminary study of multiple structures in wide ranges of their parameters it is relevant to carry out simulation. Among the types of simulation, quasistatic analysis

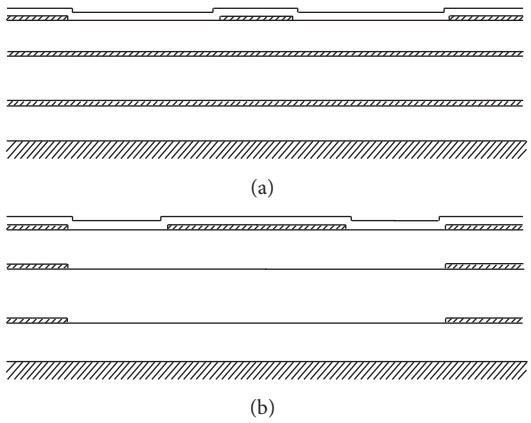

Figure 1: Microstrip line without cuts (a) and with cuts (b) in the bottom metallized layers.

(approximation based on telegraph equations, which is considered as valid only for small electrical width of a structure) [5] seems to be the most appropriate as trade-off between accuracy and computational expenses comparing to electromagnetic analysis [6]. Moreover, for particular transmission lines quasistatic analysis is quite accurate even for electrically wide structures [7] and gives results coinciding with results of measurements [8].

To explore effects of side grounded conductors, the following variants of line are considered: MSL, a microstrip line without side grounded conductors (Figure 2(a)); MSL1, a microstrip line with side grounded conductors in one (top) layer (Figure 2(b)); MSL2, a microstrip line with side grounded conductors in two (top and middle) layers (Figure 2(c)); MSL3, a microstrip line with side grounded conductors in three (top, middle, and bottom) layers (Figure 2(d)). Note that for a quasistatic calculation of parameters of a line the cross section sizes can be scaled. Therefore, from given set of size values a lot of proportional sets can be obtained. Only one set of basic sizes is considered in this paper. The geometric parameters of conductors and dielectrics are taken from the fragment of a real PCB: width of a conductor $w = 890\,\mu$m, thickness of a conductor and side grounded conductors $t = 18\,\mu$m, thickness of prepregs $h_1 = h_3 = 144\,\mu$m, and thickness of the substrate $h_2 = 220\,\mu$m (layers are numbered from the bottom up). Thickness of a solder mask is taken equal to $h_M = 30\,\mu$m and relative dielectric permittivity: of prepregs $\varepsilon_{r1} = \varepsilon_{r3} = 4.5$; of substrate $\varepsilon_{r2} = 4.4$; of solder mask $\varepsilon_{rM} = 3.5$. Width of side grounded conductors is taken equal to $5w$. Gaps between strip edges and edges of side grounded conductors in the top layer are taken equal to $s = 0.5$; 1.0; and 1.5 mm and gaps between the edges of side grounded conductors in bottom layers $(s + w + s)$.

Geometric models of four variants of the line cross section are constructed. The matrices of electrostatic and electromagnetic induction coefficients (with consideration for all side grounded conductors) are calculated by a method of moments [9] implemented in authors' software being very familiar to them and validated by electromagnetic analysis [7] and experiment [8]. Thus, proper segmentation of conductor and dielectric boundaries was the only concern, and wrong considerations caused by possible bad setup of unfamiliar electromagnetic simulators were avoided. Then, from the calculated matrices the coefficient corresponding to strip was being taken for the further calculations. At last, values of Z and τ of a line are calculated. Thus, these values take into account the effect of side grounded conductors.

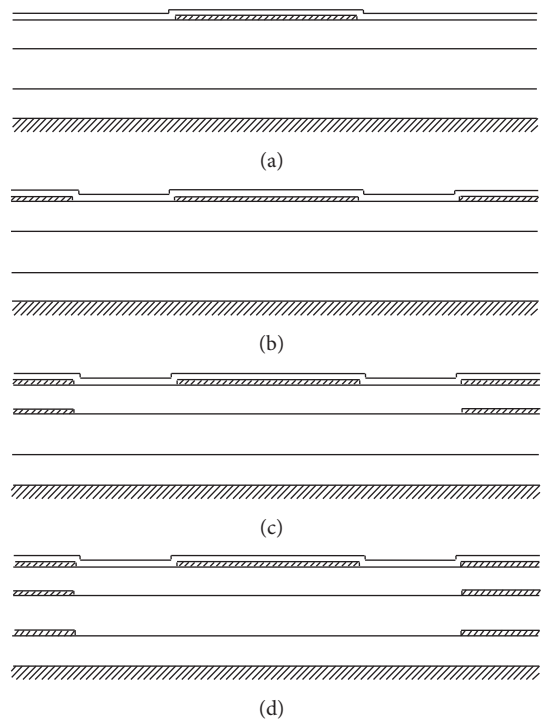

Figure 2: Cross sections: MSL (a), MSL1 (b), MSL2 (c), and MSL3 (d).

Table 1 shows values of Z and τ for different variants of structure with different distances to the side grounded conductor s. For each value a percent of deviation from a value for MSL is given.

Analysis of results for Z shows a successive decrease of its value reaching minus 0.5% for $s = 1.5$ mm, minus 1.5% for $s = 1.0$ mm, and minus 6.4% for $s = 0.5$ mm. The side grounded conductor of the top layer makes the major contribution to reduction of Z, whereas influence of the rest of the conductors is much less; in addition, the influence is diminishing when conductors are moved away from a strip. Thus the choice of the gap value is critical for Z. Only with the relatively large gaps may the presence of side grounded conductors not be taken into consideration and Z can be calculated as in an ordinary microstrip line. Reduction of gaps strongly decreases Z and requires computation of Z with consideration for side grounded conductors. It is evident that one can control Z by the amount of side grounded conductors and their gaps, if it is impossible to do by other means. Such behavior of Z can be explained by the increase in capacitance of a microstrip line; if we add side grounded conductors, it leads to the decrease for Z, according to formula $Z = 1/(v_0(C \cdot C_0)^{1/2})$, where v_0 is a light velocity in the vacuum and C and C_0 are

Table 1: Computed values of Z and τ for variants of structure with different s.

s, mm	Line	Z, Ω	ΔZ, %	τ, ns/m	$\Delta\tau$, %
1.5	MSL	50.411	0	6.098	0
	MSL1	50.167	−0.466	6.079	−0.312
	MSL2	50.155	−0.508	6.079	−0.312
	MSL3	50.152	−0.513	6.080	−0.295
1.0	MSL	50.411	0	6.098	0
	MSL1	49.731	−1.349	6.056	−0.689
	MSL2	49.681	−1.448	6.057	−0.672
	MSL3	49.668	−1.474	6.058	−0.656
0.5	MSL	50.411	0	6.098	0
	MSL1	47.614	−5.548	5.996	−1.673
	MSL2	47.280	−6.211	6.005	−1.525
	MSL3	47.190	−6.389	6.011	−1.427

per-unit-length capacitance with the given dielectrics and in the vacuum.

Analysis of results for τ shows that addition of side grounded conductors in the top layer decreases τ (down to 1.6% for $s = 0.5$ mm) and in the middle and the bottom layers, inversely, increases compensating (although not fully) the decrease of τ by the top side grounded conductors. Such behavior of τ can be explained by redistribution of electric field: in a MSL1 variant field is distributed in an external environment more than in a MSL variant. In two other variants (MSL2 and MSL3) it is distributed more in dielectrics of a line than in external environment, which leads to increase of a τ value.

It is worth noting that the presented results are obtained for particular values of PCB stack parameters; therefore, the conclusions for different values and stacks can be different. Qualitative evaluations are possible, but they are very limited. For example, one can definitely assert that, for smaller thickness of conductors (5 μm), the influence of side grounded conductors will be weaker, and for bigger thickness (35 μm) it will be stronger.

It is clear that the revealed difference of effect on Z and τ of conductors of different layers can be useful. Further we describe the microstrip line providing a desired value of Z with a stable τ at the expense of changes in corresponding gaps and constant values of width and thickness of a signal conductor, thickness, and ε_r of the substrate [3]. The line contains a strip and a reference ground plane, a dielectric substrate, and it differs from an ordinary microstrip line by presence of solid conductive areas, which are placed in the same level as a signal conductor and in the level below it. A useful result is achieved by selection of values of gaps between side grounded conductors in the way to obtain a defined decrease of the value of Z with the constant value of τ at the expense of simultaneous narrowing of gaps in the top and bottom layers. Constancy of τ is being provided by its value decreasing with a decrease of gaps, which are in the same level as a strip, and increasing with a decrease of a gap under the strip.

To verify the considerations above by quantitative evaluations, modelling of a microstrip line with two layers (Figure 3(a)) is carried out. The first layer with thickness h_1 and dielectric permittivity of a dielectric ε_{r1} contains only side grounded conductors with thickness t and gap between them is s_1. The top layer with thickness h_2 and relative dielectric permittivity of a dielectric ε_{r2} contains microstrip with thickness t and width w and side grounded conductors with thickness t and gaps s_2. Per-unit-length delay τ of a transmission line depends on a distribution of field in dielectrics. If the value ε_r of layers is more than that of the environment in which the line is, the τ value decreases with reduction of s_1, because the field distribution in the external environment is increasing. Reduction of s_2 leads to increase of the τ value, because field is being distributed in the dielectrics of a structure is increasing. Thus, it is possible to obtain stable value of τ at the expense of a compensation for its change by one gap by change of another gap.

Figure 3(b) shows dependency diagrams of τ on s_1 for $s_2 = 0.89$; 1.09; 1.29; and 1.49 mm. From these diagrams we can see that different combinations of values s_1 and s_2 provide the same τ (values close to 5.8 ns/m are marked). Figure 3(c) shows similar diagrams for value of Z. It can be seen that if combinations satisfy a condition of constancy of τ, the value of Z changes.

Despite only one considered set of basic parameters of conductors and dielectrics, the revealed phenomenon of the opposite influence of top and bottom gaps for capacitance of a line is general. Therefore, a desirable result can be obtained by similar way for other parameters by everyone interested, using a proper simulation. Thus, according to the examined influence, it is possible to create a microstrip line, the characteristic impedance and the delay of which would be controlled by selection of distance to side conductors in the top and bottom layers. Moreover, the sensitivity of such line delay to parameter variations can be less. For example, the foil etching process during the PCB manufacturing increases gaps between conductors. However, the simultaneous increasing of the gaps in the top and bottom layers will oppositely influence the delay, thus decreasing the resulting sensitivity.

Proper usage of the proposed approach can considerably simplify the achievement of strict requirements to wireless

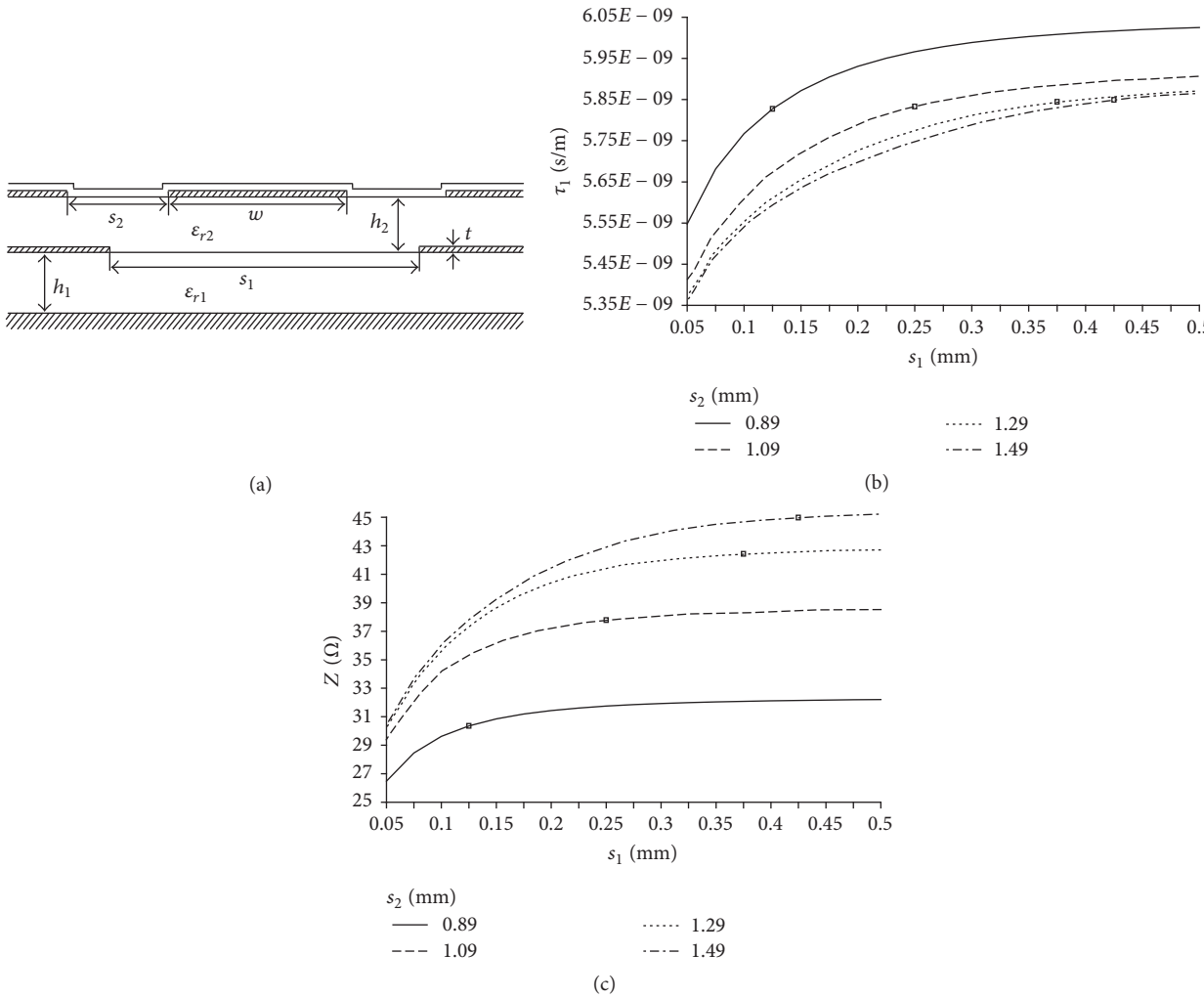

Figure 3: Cross section of a microstrip line with side grounded conductors (a), its per-unit-length delay (b), and characteristic impedance (c).

communications equipment. Particularly, it can be applied to the group delay in the high-frequency analog circuits of global navigation systems. Another application is the timing problem in high-speed digital circuits of data processing systems.

Competing Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

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References

[1] T. R. Gazizov and N. A. Leontiev, "Reduction of high-speed signal distortions in double-layered dielectric PCB interconnects," in *Proceedings of the 6th Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 67–69, October 1997.

[2] T. R. Gazizov, "Far-end crosstalk reduction in double-layered dielectric interconnects," *IEEE Transactions on Electromagnetic Compatibility*, vol. 43, no. 4, pp. 566–572, 2001.

[3] V. K. Salov and T. R. Gazizov, "Simulation of a microstrip line with polygons," *Dokladi TUSUR*, vol. 3, no. 29, pp. 162–164, 2013 (Russian).

[4] V. K. Salov, T. R. Gazizov, and A. M. Zabolotsky, Patent 2584502 of Russian Federation. Microstrip line with stable delay, 2016.

[5] A. R. Djordjević, T. K. Sarkar, and R. F. Harrington, "Time-domain response of multiconductor transmission lines," *Proceedings of the IEEE*, vol. 75, no. 6, pp. 743–764, 1987.

[6] K. Wu, "Electromagnetic analysis of multiconductor losses and dispersion in high-speed interconnects," *Analog Integrated Circuits and Signal Processing*, vol. 5, no. 1, pp. 47–56, 1994.

[7] P. Orlov, T. Gazizov, and A. Zabolotsky, "Short pulse propagation along microstrip meander delay lines with design constraints: comparative analysis of the quasi-static and electromagnetic approaches," *Applied Computational Electromagnetics Society Journal*, vol. 31, no. 3, pp. 238–243, 2016.

[8] A. T. Gazizov, A. M. Zabolotsky, and T. R. Gazizov, "UWB pulse decomposition in simple printed structures," *IEEE Transactions on Electromagnetic Compatibility*, vol. 58, no. 4, pp. 1136–1142, 2016.

[9] T. R. Gazizov, "Calculation of a capacitance matrix for a two-dimensional configuration of conductors and dielectrics with orthogonal boundaries," *Russian Physics Journal*, vol. 47, no. 3, pp. 326–328, 2004.