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A Software Designed to Generate Transistor Models with Interconnections

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***Abstract*—In this paper, an algorithm is developed to generate a transistor model that takes into account parasitic parameters of its interconnections. The algorithm includes the following steps: determining parasitic parameters of the transistor footprint and interconnections on the PCB and inside its enclosure, and setting the parameters of the SPICE-model of the transistor crystal. Based on this algorithm, a graphical interface of the program module for creating augmented transistor models has been developed. The models take into account parasitic parameters of its interconnections that depend on a particular radio-electronic device to be developed. To verify the model, we created an augmented model of the BFR91A bipolar transistor. Applying this model, we built a model of an oscillator circuit and simulated this circuit using the transistor model provided by its manufacturer. The augmented model significantly reduced the voltage amplitude at the output of the oscillator (by 7.38 dB) and increased the oscillation start-up time (from 2 to 9 μs). This indicates that the augmented transistor model provides simulation results that reflect its behavior under real-world operating conditions.**

***Keywords*—SPICE-model, electronic components, simulation, transistor, software module**

I. Introduction

Design of modern radioelectronic equipment is performed in stages and contains simulation with the use of various programs and tools. The tools based on SPICE-simulation (Simulation Program with Integrated Circuit Emphasis) are widely used in the development of electrical circuits [1]. In these tools, the models of *RLC*-components can be represented taking into account their parasitic parameters [2]. An important condition in simulation is the use of models that can correctly describe the characteristics of real electronic components (ECs). Creating such models is a challenging task, especially for models of semiconductor ECs. Traditionally, semiconductor ECs are described using widely known models. For example, a model based on the Shockley equation [3] is used to simplify the description of a semiconductor diode. The Ebers-Moll [4] and Gummel-Poon [5] models are used for bipolar junction transistors (BJTs), and the Shichmann-Hodges [6] and BSIM [7] models – for field-effect transistors (FETs). These models are relatively simple and their validity is sufficient for the preliminary simulation phase of electrical circuit simulation. However, improving the performance of digital circuits and operating frequencies of analog circuits requires taking into account the influence of many parasitic parameters. For this purpose, the EC models can be customized by adding additional parasitic parameters. For example, in [8], the Gummel-Poon model is modified to derive a behavioral model for silicon carbide (SiC) based BJTs. In [9], the BSIMSOI and EKV-SOI models [10] are modified to obtain a FET model considering ionizing radiation. In addition, nowadays, models are obtained by applying completely new approaches. For example, in [11], the diode model is obtained using neural network, and in [12], the application of neural network improved the FET model.

Most semiconductor EC models do not consider the effects of the footprint and interconnections on printed circuit boards (PCBs), as well as the interconnections between the crystal and electrodes inside the EC enclosure. This often causes difficulties for designers when developing radio-electronic equipment, in particular, when ensuring signal and power integrity. For example, in [13] it is shown that, considering the applied solder layer, the EC footprint can lead to the occurrence of parasitic capacitance, significantly affecting EC electrical parameters. A technique for simulating passive electric circuits [14] enabled taking into account some EC parasitic parameters. However, its application to semiconductor ECs is not foreseen. Hence, it is important to develop tools for creating transistor models that allow considering parasitic parameters of PCB interconnections, footprints and electrodes, as well as interconnections located inside the enclosure.

The purpose of this work is to develop a software module for creating transistor models that take into account parasitic parameters of their interconnections.

II. Algorithm for Creating an Augmented Transistor Model

Creating an augmented transistor model involves six steps (Fig. 1). In the first four steps, the parameters of the model are determined, and in the last steps the structure of the model is formed.

In the first step, we define the mathematical description of the transistor crystal model (e.g., the Gummel-Poon model for BJTs or the Shichman-Hodges model for FETs, etc.) and specify its parameters. The extraction of the crystal model parameters can be done by the developer himself [15], or an existing SPICE-model of the transistor can be used. The crystal

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model is the basis for creating the augmented model, so its choice determines the validity of the modeling results.

In the second and third steps, the selected transistor crystal model is supplemented with parasitic parameters (capacitance and inductance) of the EC footprint on the PCB, as well as parasitic parameters of the electrodes and interconnections inside the enclosure. In some crystal models, parasitic parameters of electrodes are often taken into account, so it is enough to consider the influence of the footprint only.

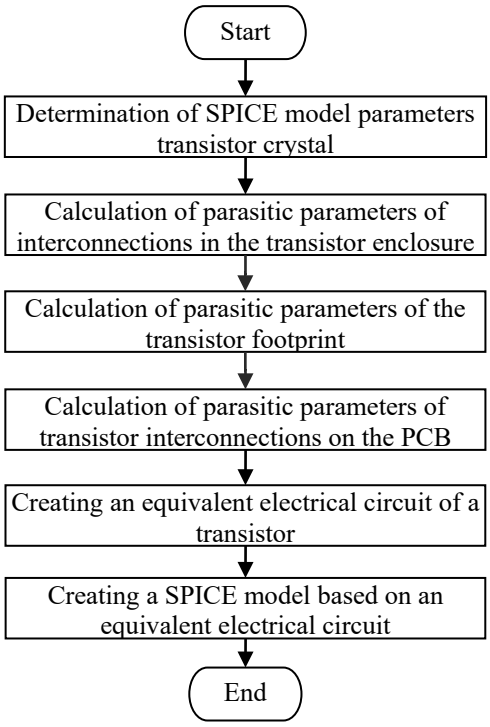

Fig. 1. The algorithm for creating an augmented transistor model.

In the fourth step, we consider the influence of the PCB interconnections connected to the EC electrodes. For each conductor connected to the EC electrodes, the capacitance and inductance are calculated. For simple cross sections of PCB interconnections (microstrip [16] and stripline [17] transmission lines), they can be calculated analytically, with an acceptable error. Such calculations can be performed in the initial stages of design when the PCB stack is not fully defined. Numerical methods such as the method of moments (MoM) [18] are used for complex cross-sections of PCB interconnections.

In the next step, we generate an equivalent circuit that contains a crystal model, capacitances, and inductances as concentrated elements to account for parasitic parameters introduced by the footprint and PCB interconnections.

In the final step, ports and logic symbols are assigned, which allows the equivalent circuit to be simulated as a single element. This solution reduces the total number of elements in the circuit, thus simplifying its understanding.

III. Graphical Interface of the Software Module for Creating Augmented Transistor Models

Based on the algorithm (Fig. 1), a software module was developed to create transistor models that take into account parasitic parameters of their interconnections. First, the user needs to enter the parameters of the SPICE-model of the crystal or import a ready-made SPICE-model. The dialog box for setting the parameters of the crystal SPICE-model in the software module is illustrated in Fig. 2.

Then, parasitic parameters of the EC footprint are calculated. The software module contains a database of footprint for standard EC enclosures, which can be edited by the user if necessary. Thus, the EC enclosure and its respective footprint are selected, and the capacitance and inductance are calculated for the selected footprint. The dialog box for specifying the geometrical parameters of the EC footprint is illustrated in Fig. 3.

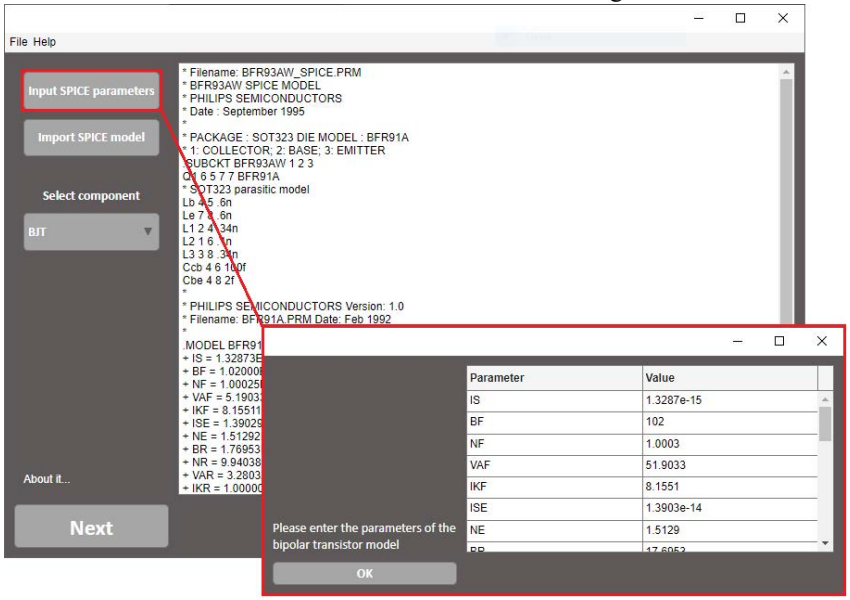

Fig. 2. The dialog box for setting the parameters of the crystal SPICE-model.

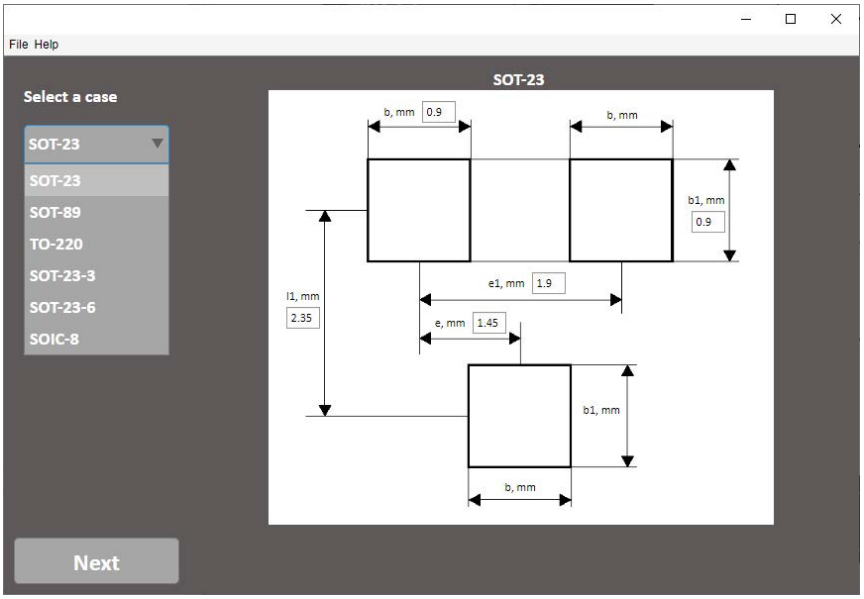

Fig. 3. The dialog box for setting the geometrical parameters of the EC footprint.

Further, the parasitic parameters of the interconnections connected to the EC footprint are entered into the model. For this purpose, the user selects or creates a cross-sectional model of the interconnection. The electrical parameters of the cross section selected from the built-in database are calculated analytically. For user-constructed cross sections, calculations are performed using the MoM. The results of the calculations are the capacitance and inductance values of these interconnections. The dialog box for creating a cross-sectional model of EC interconnections on the PCB is illustrated in Fig. 4.

In the final step, an equivalent circuit is generated based on the obtained elements (transistor crystal model and parasitic capacitances and inductances) using SPICE syntax. The resulting equivalent circuit is saved in a text form as a single model that the user can integrate into the library of a SPICE simulation program.

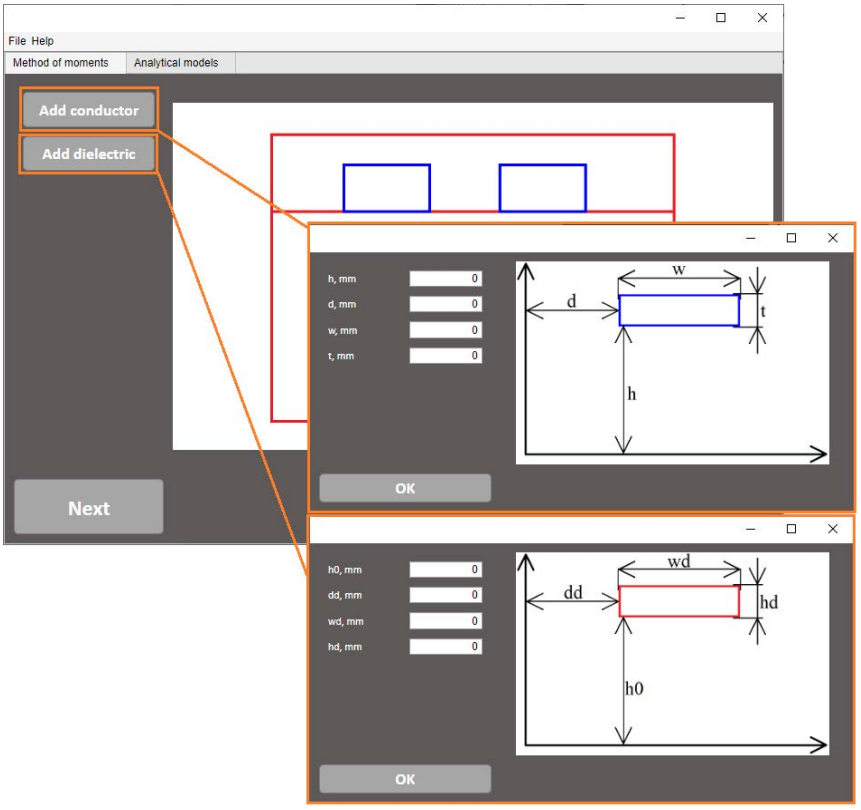

Fig. 4. The dialog box for creating a cross-sectional model of EC interconnections on PCBs.

IV. Application of the Augmented Model in Electrical Circuit Simulation

The obtained augmented transistor model was applied in the electrical circuit of the oscillator according to the Klapp circuit (Fig. 5) operating at a frequency of 433 MHz. Resistors $R1 = 2.49$ kΩ and $R2 = 24.9$ kΩ determine the operating point for transistor $T1$ (BFR91A). Capacitor $C1 = 3.9$ nF is the power filter. The bypass choke $L1 = 100$ nH and resistor $R3 = 12$ Ω do not allow the variable component of the excited oscillations to influence the bias and power supply circuits. The correction circuit $C3 = 10$ pF and $R4 = 2.49$ Ω allows to compensate the phase shift between the first harmonic of the collector current and the control voltage on the base. The auto bias circuit $C4 = 120$ pF and $R5 = 33$ Ω allows the cutoff angle to be reduced when the generation mode is reached. The frequency of the oscillator is determined by the oscillating circuit: $L4 = 33$ nH, $C5 = 4.3$ pF, $C6 = 120$ pF, and $C8 = 150$pF. The decoupling capacitor $C7 = 6$ pF cuts off the constant current component from the output. The oscillator load is resistor $R6 = 50$ Ω.

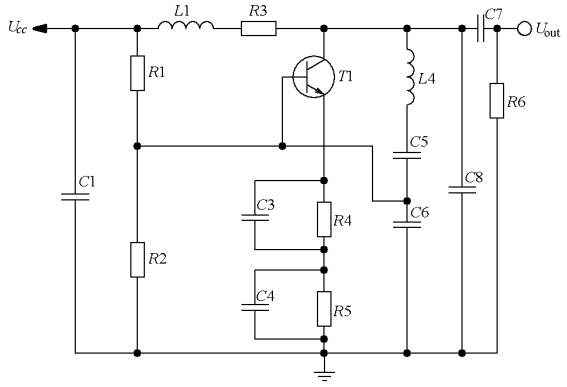

Fig. 5. The electrical circuit of the oscillator.

If the connections of the electrodes of transistor $T1$ with the elements of the electrical circuit are made in the form of microstrip transmission lines (Fig. 6), with parameters (Table I.), then the line capacitance will be equal to 0.245 pF, and inductance – 3 nH.

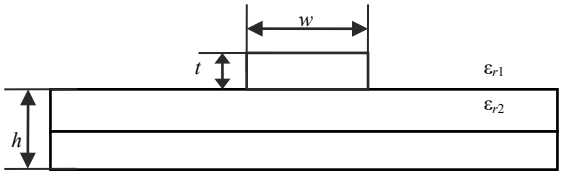

Fig. 6. The cross-section of a microstrip transmission line.

For 433 MHz, an inductance of 3 nH will provide a reactance on the order of 11.4 Ω, which is comparable to the resistance $R5$ in the auto-biasing circuit. The presence of such a resistance in the emitter circuit can significantly affect its operation. In addition, the capacitance of the base-emitter p-n junction of the BFR91A transistor is about 1.5 pF, and the inductance of the base electrode for the SOT-32 enclosure is about 0.6 nF. As a result, the PCB interconnections, the base electrode, and the p-n junction capacitance form an oscillating circuit, with an oscillation frequency of 2 GHz. Such fluctuations in transistor base current can destabilize the oscillator. The augmented transistor model allows the resulting parasitic capacitances and inductances to be accounted for in the simulation. The equivalent circuit of the resulting augmented model of BJT $T1$ (Fig. 7) contains inductance elements L_{bline}, L_{cline}, L_{eline} and capacitances C_{bline}, C_{cline}, C_{eline} at each electrode of the BJT. The ratings of these elements refer to the values of the parasitic inductance and capacitance of the interconnections connected to its electrodes (3 nH and 0.245 pF).

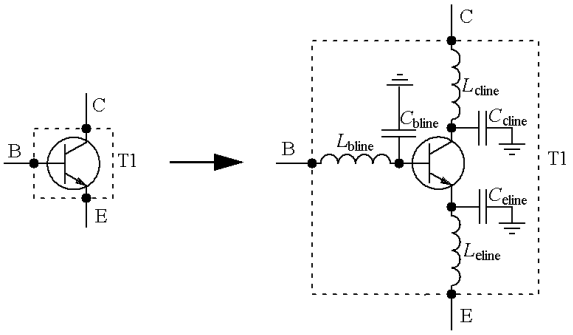

Fig. 7. The equivalent circuit of the augmented BJT model.

The oscillator was simulated with the obtained augmented BJT model, as well as with the model provided by the manufacturer. The simulation results were oscillograms of the voltage U_{out} at the oscillator output (Fig. 8).

TABLE I. The Parameters of the Cross-Section of a Microstrip Transmission Line

Parameters	Value
conductor width (w), mm	0.5
metallization thickness (t), μm	35
substrate thickness (h), mm	1.8
relative vacuum dielectric constant (ε_{r1})	1.0
relative substrate dielectric constant (ε_{r2})	4.5
length (l), mm	5.0

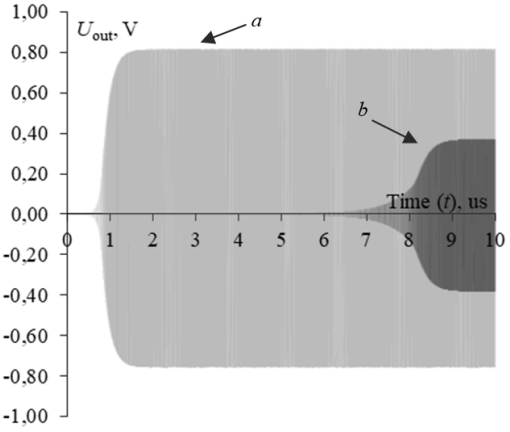

Fig. 8. The oscillograms of the voltage at the oscillator output: with the manufacturer's BJT model (*a*), with the augmented BJT model (*b*).

It can be seen from Fig. 8 that when the augmented transistor model was applied, the voltage amplitude at the oscillator output decreased by a factor of 2.34 (or 7.38 dB). This significant decrease in amplitude can be explained by the presence of additional reactance in the autocoupling circuit in

the circuit with the obtained model. At the auto oscillation frequency (433 MHz), this resistance led to a slight decrease in the cutoff angle of the transistor and the amplitude of the output voltage. In addition, Fig. 8 shows that the oscillation start-up time for the circuit with the obtained model increased from 2 to 9 μs. To evaluate the frequency properties of the oscillator circuit, the amplitude spectra of the U_{out} voltage were obtained (Fig. 9).

Fig. 9 illustrates that the application of the augmented transistor model significantly attenuated the level of signal components at the oscillator output. The magnitude of attenuation of the components below the operating frequency was about 25 dB, and for the components above the operating frequency it was 19 dB.

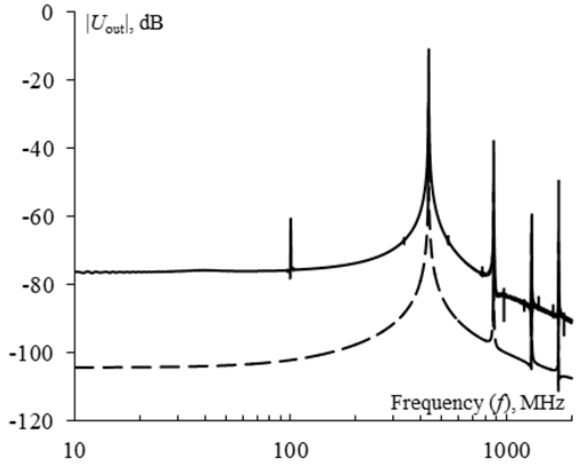

Fig. 9. The voltage spectra of the oscillator U_{out} with manufacturer's model (——)and with augmented (- - -) BJT model.

V. Conclusion

An algorithm has been developed to determine parasitic parameters of the transistor footprint, the interconnections on the PCB and inside its enclosure, as well as to adjust the parameters of the SPICE-model of the transistor crystal. Based on the algorithm, a graphical interface software module was developed to create transistor models that take into account parasitic parameters of its PCB interconnections. The result of the software module is a generated augmented SPICE-model of the transistor. The distinctive feature of this model is that it allows considering parasitic parameters of transistor interconnections for a particular device to be developed.

We have also built an augmented model of the BFR91A BJT that takes into account parasitic parameters of its interconnections on the PCB. The oscillator on the BFR91A BJT operating at 433 MHz was simulated using the obtained augmented model and the model provided by the manufacturer. Simulations showed that the application of the augmented model significantly reduced the voltage amplitude at the output port of the oscillator (by 7.38 dB) and increased the oscillation start-up time from 2 to 9 μs. This increase might have been caused by the influence of parasitic parameters of the PCB interconnections on the BJT operation. The reactance of the conductor connected to the BJT emitter at 433 MHz was about 11.4 Ω, which resulted in a slight decrease in the cutoff angle of the transistor. Therefore, we can conclude that when simulation electrical circuits operating at high and ultrahigh frequencies, it is necessary to use augmented transistor models that consider parasitic parameters of their interconnections.

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