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Influence of Conductor Arrangement on Different Layers of the Printed Circuit Board Under its Exposure to Electrostatic Discharge

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***Abstract*—The paper analyzes self- and mutual capacitances of fragments of two-layer printed circuit boards (PCBs) based on microstrip (MTL), coupled (CTL), and coplanar (CopTL) transmission lines (TLs) when the distance between conductors is changed. It is shown that increasing the substrate thickness by a factor of 10 leads to a 2-fold decrease in the self-capacitance with perpendicular and 7.4-fold decrease with parallel conductor arrangements in the MTL-based models. Increasing the substrate in CTL-based models leads to a decrease in self and an increase in mutual capacitance. For CopTL, increasing the substrate thickness leads to a decrease in the self and mutual capacitance with perpendicular arrangement of conductors. Parallel conductor arrangement leads to an increase in the self and mutual capacitance. We have also analyzed the influence of conductor arrangement when the PCB is exposed to electrostatic discharge (ESD). For the MTL-based models, perpendicular arrangement of conductors leads to a decrease in the crosstalk at the near end by 8 times, and at the far end - by 5.5 times. The perpendicular arrangement of the CopTL conductors reduced the near-end crosstalk by a factor of 35 and the far-end by a factor of 8. Analysis of the CTL-based PCB showed that the perpendicular arrangement of conductors leads to an increase in the crosstalk on a passive conductor located on the same layer as the active one by 1.5 times. However, the crosstalk on conductors located on the opposite layer decreased by 9.3 times at the near end, and by 6.6 times at the far end. Thus, when designing radio electronic equipment, it is necessary to take into account these features of the location of conductors to increase its resistance to electromagnetic interference. The developed models can be used in a comprehensive analysis of electronic components of radio electronic equipment under the destabilizing ESD impact.**

Keywords—electromagnetic compatibility, self-capacitance, mutual capacitance, printed circuit board, transmission line, electrostatic discharge, crosstalk

I. Introduction

The analysis of the design and arrangement of conductors on a printed circuit board (PCB) is necessary to ensure electromagnetic compatibility (EMC) [1]. Increasing the degree of integration of electronic components and the use of surface mount technology has allowed the size of devices to be reduced. However, the density of components on the PCB has increased, leading to an increase in inductive and capacitive coupling between conductors [2, 3]. As a result, the sensitivity of radio electronic equipment (REE) to external and internal electromagnetic interference (EMI) increases, which can lead to irreversible and catastrophic failures [4]. One such source of EMI is electrostatic discharge (ESD) [5]. Resistance to ESD impact is determined at the stage of REE design. For example, in [6] it was revealed that an increase in the PCB capacitance leads to an increase in the sensitivity of the transistor when it is exposed to ESD. In [7], it was shown that capacitive coupling between the electrodes of a transistor increases its sensitivity to ESD by 10%.

In [8], it was proposed to use multilayer PCBs to minimize mutual inductive and capacitive coupling. In the meantime, the conductors are arranged on one or several layers of the PCB. Each PCB can be represented as: microstrip (MTL), coplanar (CopTL) or coupled (CTL) transmission lines (TLs). In addition, the arrangement of the conductors relative to each other can be at different angles (from 0 to 90º) on different layers of the PCB. In this case, the mutual capacitive and inductive electromagnetic couplings will depend on the electrical and geometric parameters of the conductors and dielectrics of the interconnection. For example, the analysis of a two-layer PCB for on-board spacecraft equipment [9] showed that optimal changes of electrical and geometrical parameters of the PCB conductors allows reducing the inductance up to 10 times. It was also shown that increasing the distance between the conductors by 10 times led to an increase in the conductors self-capacitance by 1.3 times and a decrease in the conductors mutual capacitance by 12.7 times.

As a result, it is recommended to estimate the amplitudes of crosstalk on conductors located on different layers of the PCB under the ESD exposure. The estimation will allow taking into account parasitic coupling in PCB design and reducing the ESD impact on REE electronic components.

The purpose of this work is to evaluate the influence of the arrangement of conductors on different layers of the PCB when it is exposed to ESD.

II. Development of Two-Layer PCB Models

To estimate the self and mutual capacitances of conductors located on different layers of the PCB, we took the MTL, CTL and CopTL models as a basis. In this case, the values of the geometric parameters of width (w), conductor thickness (t), its

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height above the conductor grounded (glass-fiber thickness) (h) and its length (l) were calculated for a given characteristic impedance (Z_C) equal to 50 Ohms with a dielectric constant (ε_r) substrate equal to 4.5. For the MTL, the following values were obtained: $w = 3.256$ mm, $t = 35$ µm, h=1.6 mm, and $l = 50$ mm. For the CTL: $w = 3.256$ mm, h=1.6 mm, $t = 35$ µm, $l = 50$ mm, and the conductor spacing (s) of 2.5 mm. For the CopTL: $w = 2.65$ mm, h=1.6 mm, $t = 35$ µm, $l = 50$ mm, and the distance between the active and grounded conductors (s_1) was 0.8 mm. Based on the obtained values, geometric models of two-layer PCB fragments were created (Fig. 1). When creating fragment models, the conductors were mirrored parallel and perpendicular to the opposite layer. As a result, we created the MTL-based fragments (Fig. 1 (a, b)), the CTL-based fragments (Fig. 1 (c, d)), and the CopTL-based fragments (Fig. 1 (e, f)). In the developed models based on MTL and CTL, the added (bottom) conductors are grounded. In the CopTL-based models, the grounded conductors were placed laterally on both layers of the PCB.

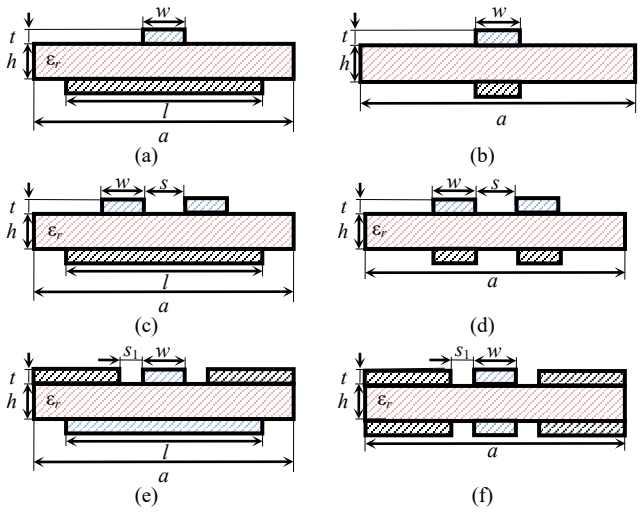

Fig. 1. Geometric models of PCB fragments with conductors located perpendicularly (a, c, e) and in parallel (b, d, f)

3D-models of the PCB fragments were constructed (Fig. 2) using the MOM3D module in the TALGAT software [10], which is based on the method of moments (MoM).

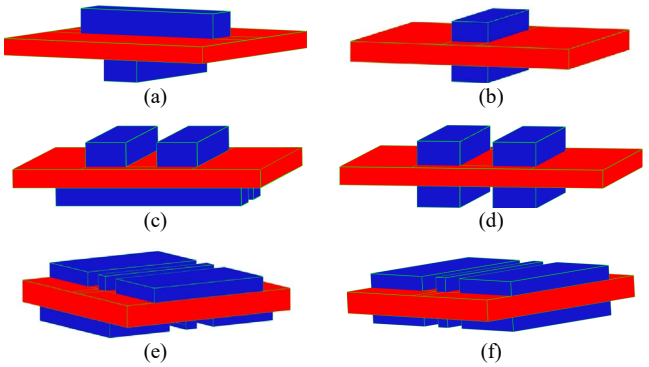

Fig. 2. 3D-models with perpendicular (a, c, e) and parallel (b, d, f) conductors for PCB fragments based on MTL (a, b), CTL (c, d), and CopTL (d, f)

Module is designed for electrostatic analysis of three-dimensional structures and enables calculating the matrix of electrostatic induction coefficients (**C**) with a given dielectric filling.

III. Calculation Results of Capacitive Matrix

The TALGAT software calculated the elements **C** of the PCB fragment models (Fig. 2) when h changed from 0.2 to 2 mm. These dimensions imitate the real PCB thickness. Since the MTL-based model is represented as one active and one grounded conductor, matrix **C** has one element, which is the self-capacitance (C) of the conductor. To verify the results, similar calculations were performed using the finite element method (FEM). The dependences of C on h obtained by two methods for perpendicular and parallel conductors are shown in Fig. 3.

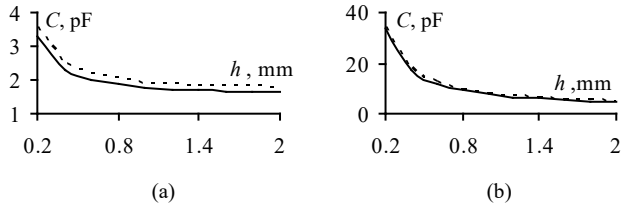

Fig. 3. Relationship between C and h for perpendicular (a) and parallel (b) conductor arrangement calculated with MoM (—) and FEM (- - -)

The analysis showed that when h was increased from 0.2 to 0.4 mm, C values decreased by 1.4 (from 3.28 to 2.32 pF) for perpendicular and by 1.9 (from 33.8 to 17.5 pF) for parallel conductor arrangement. Increasing h from 0.4 to 2 mm led to a decrease in C values by a factor of 1.4 (from 2.32 to 1.64 pF) for perpendicular and by a factor of 3.8 (from 17.5 to 4.6 pF) for parallel conductor arrangement. Moreover, for the structures with perpendicularly located conductors, at $h = 0.2$ mm, the C value was 10.3 times less than for a parallel one, and at $h = 2$ mm, it was 2.8 times less. The maximum differences (δ) of the calculated results using the MoM and the FEM were 8.8% and 5.8% for perpendicular and parallel conductors, respectively.

Similar calculations were performed for the CTL-based models. Since in the models the two lower conductors are grounded, the **C** elements were calculated for the two upper conductors. The diagonal elements of the capacitance matrix (self-capacitance of the first C_{11} and second C_{22} conductors) were calculated as the sum of the electrostatic induction matrix elements by row. The off-diagonal elements of the capacitance matrix (mutual capacitances $C_{12} = C_{21}$) are equal to the off-diagonal C elements with the opposite sign.

Fig 4 depicts the calculated values of the self (C) and mutual (C_m) capacitances for the CTL. Fig. 4 shows that with perpendicular arrangement of conductors, an increase in h leads to a decrease in C by 3.6 times (from 5.4 to 1.5 pF) (Fig. 4 (a)), and with a parallel arrangement – by 7.7 times (from 33.9 to 4.4 pF) (Fig. 4 (b)). It is worth noting that the C_m values increase by 1.7 times (from 0.6 to 1.1 pF) with perpendicular (Fig. 4 (c)) and by 2.3 times with parallel (Fig. 4(d)) conductors. Additionally, the C_m with perpendicular conductor arrangement is twice as big as with parallel

arrangement. In the meantime, δ values do not exceed 9.2% for perpendicular conductors and 8.9% for parallel conductors.

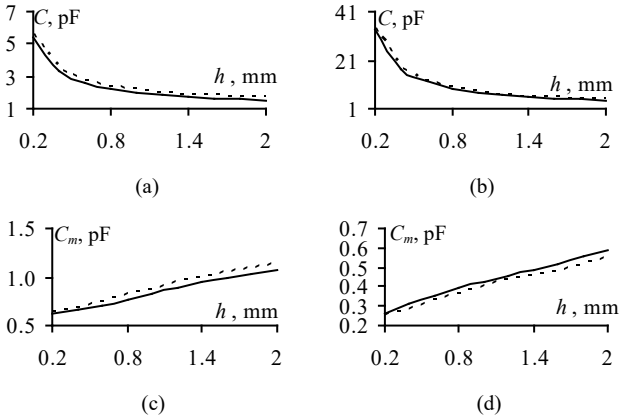

Fig. 4. Relationships between C (a, b) and C_m (c, d) and h for perpendicular (a, c) and parallel (b, d) conductor arrangement calculated with MoM (– –) and FEM (- - -)

The values of self and mutual capacitances for the CopTL-based models were calculated similarly (Fig. 5).

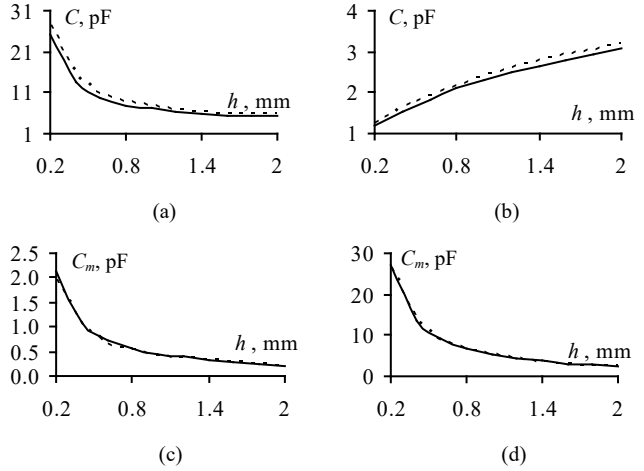

Fig. 5. Relationships between C (a, b) and C_m (c, d) and h for perpendicular (a, c) and parallel (b, d) conductor arrangement calculated with MoM (– –) and FEM (- - -)

The analysis showed that when h increases, the values of C increase by 2.6 times (from 1.18 to 3.06 pF) (Fig. 5(b)) and decrease by 4.9 times (from 25.3 to 5.1 pF) (Fig. 5(a)). In this case, the C_m values decrease by 11.5 times (from 27.1 to 2.36 pF) with parallel (Fig. 5(d)) and by 10.6 times (from 2.12 to 0.2 pF) with perpendicular (Fig. 5(c)) arrangement of conductors. Note that for self-capacitances, an increase in h leads to a decrease in the case of perpendicular and an increase in case of parallel arrangement of the conductors of the CopTL. In this case, the differences in δ do not exceed 9.7% for perpendicular and 5.6% for parallel arrangement of conductors of the CopTL.

IV. ESD Impact Analysis

Next, we analyzed the influence of the location of conductors on the crosstalk when the PCB is exposed to ESD. Fig. 6 shows a schematic diagram of the ESD impact on the MTL and the CopTL. Its voltage waveform according to [11] is shown in Fig. 7. The crosstalk on the MTL-based two-layer PCB (Fig. 1 (a, b)) was analyzed under the condition that the upper conductor was active and the lower one was passive. In addition, the ground layer was placed at a distance of 0.1 m to minimize its influence.

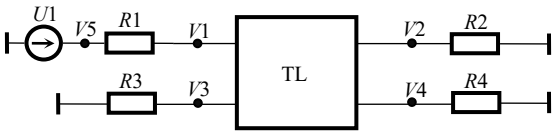

Fig. 6. Schematic diagram of the ESD impact on the TL

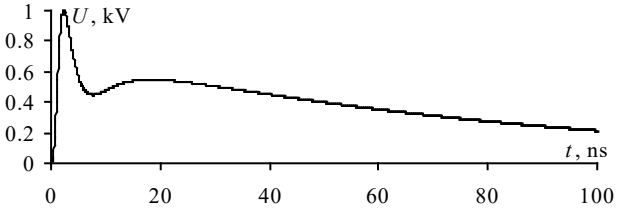

Fig. 7. Voltage waveform at node $V5$

The voltage waveforms at the beginning ($V3$) and end ($V4$) of the passive conductor for the MTL-based PCB fragment at $h = 1.6$ mm are shown in Fig. 8 (a, b). The crosstalk amplitude dependences when h is changed from 0.2 to 2 mm are shown in Fig. 8 (c, d). Fig. 8 (a) shows that the crosstalk at nodes $V3$ and $V4$ with perpendicular conductors is the same and equals 24.4 V. The crosstalk with parallel conductor arrangement at node $V3$ is 176.5 V and at node $V4$ it is 131.4 V (Fig. 8 (b)).

The dependence in Fig. 8 (c) shows that increasing h (from 0.2 to 0.4 mm) leads to a 1.4-fold decrease in amplitude (from 53.2 to 36.7 V). When h is increased to 2 mm, the crosstalk decreases by 1.5 times (from 36.7 to 23.9 V). This indicates that components on a two-layer PCB with a thin ($h = 0.2$ mm) dielectric layer are more vulnerable (1.4 times) to ESD than components on a PCB with a dielectric layer that is twice as large. As a result, the crosstalk on the MTL-based fragment depends on C between the two conductors (Fig. 3). The worst case occurs with parallel conductors. Thus, increasing h leads to attenuation of the crosstalk amplitude at node $V3$ by 1.9 times and increase at node $V4$ by 3.3 times (Fig. 8 (b)). As a result, at $h = 0.2$ mm, the crosstalk at node $V3$ with perpendicular conductor arrangement is 5.8 times smaller than with parallel arrangement, and at node $V4$ it is 1.3 times larger. However, when $h = 2$ mm, the crosstalk at node $V3$ is 6.8 times smaller and at node $V4$ – 5.3 times smaller.

Fig. 9 shows the waveforms of the crosstalk voltage depending on h for the CopTL-based fragment. Fig. 9 (a) shows that, with perpendicular arrangement of conductors, the crosstalk at nodes $V3$ and $V4$ is the same and does not exceed 1.9 V at $h = 1.6$. However, the parallel arrangement of conductors leads to an increase in the crosstalk at node $V3$ by 34.4 times and at node $V4$ by 7.5 times (Fig. 9 (b)). Fig. 9 (c) shows that increasing h reduces the crosstalk at nodes $V3$ and $V4$ by 6 times. In the meantime, at node $V3$, the parallel arrangement of conductors reduces crosstalk by 4.3 times, and at node $V4$ – by 10.9 times (Fig. 9 (d)). Perpendicularly placed conductors attenuate crosstalk at node $V3$ by 35 times and at node $V4$ by 8 times.

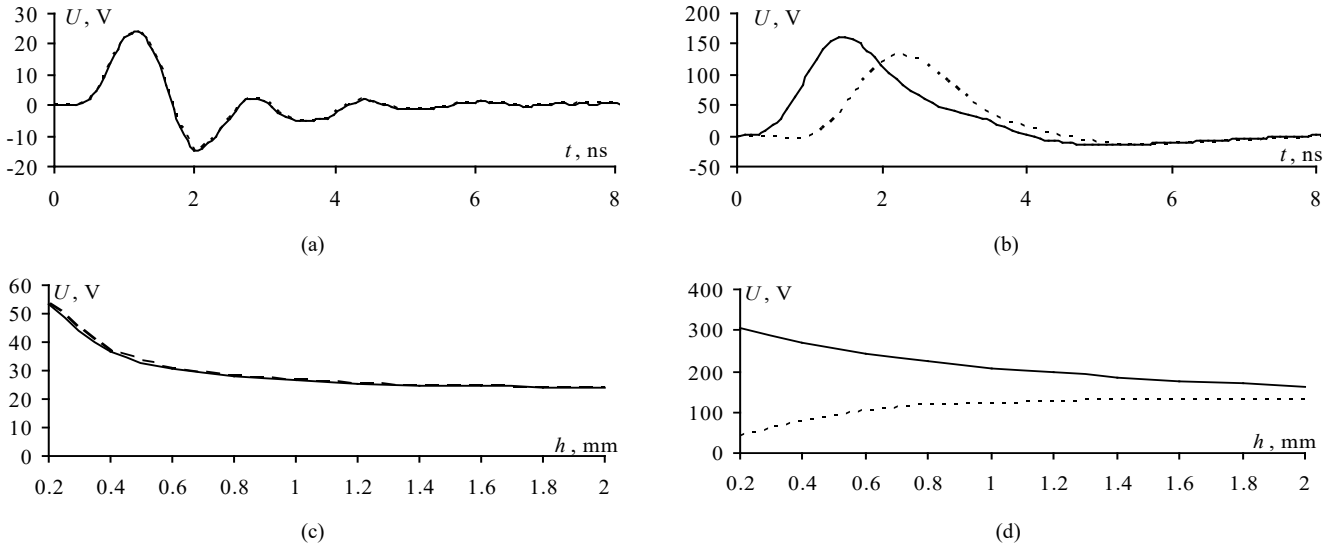

Fig. 8. Voltage waveforms at nodes *V*3 (—) and *V*4 (- -) and relationship between the amplitude and *h* under the ESD impact on the MTL with perpendicular (a, c) and parallel (b, d) conductor arrangement

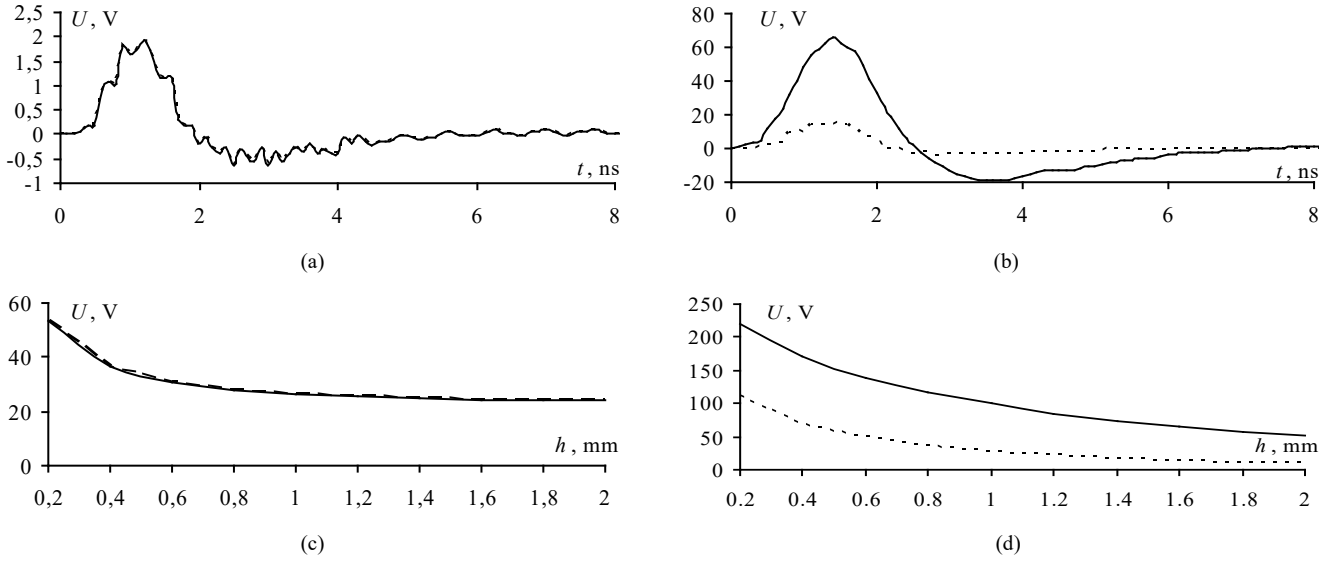

Fig. 9. Voltage waveforms at nodes *V*3 (—) and *V*4 (- -) and relationship between the amplitude and *h* under the ESD impact on the CopTL with perpendicular (a, c) and parallel (b, d) conductor arrangement

The crosstalk in the CTL-based fragment (Fig. 1 (c, d)) was analyzed under the condition that one of the upper conductors was active and the rest were passive. In this case, the distance to the ground plane was 0.1 m. Fig. 10 shows a schematic diagram of the ESD impact. Line *V*3-*V*4 imitates the conductor located on the same layer as the active conductor. When the conductors are parallel, line *V*5-*V*6 imitates the passive conductor located on the opposite layer under the active conductor, and *V*7-*V*8 imitates the conductor located under the passive one.

Fig. 11 (a, b) shows the voltage waveforms at nodes *V*3 and *V*4 at $h = 1.6$ mm. Fig. 11 (c, d) depicts the relationship between the maximum crosstalk and *h*. Fig. 11 (a) shows that the crosstalk at nodes *V*3 and *V*4 does not exceed 75.1 and 93 V, respectively. In this case, with parallel conductors at *V*3 and *V*4 nodes, the crosstalk is the same (63.5 V), but has different polarity. Increasing *h* between perpendicular conductors leads to a 1.3 times decrease in crosstalk at node *V*4 (from 121.3 to 90.9 V). At node *V*3, the crosstalk decreases when *h* is increased to 1 mm. Further increase leads to a slight increase in crosstalk (from 72.6 to 76.9 V). The crosstalk at *V*3 and *V*4 nodes increases (from 60 to 65 V) when the conductors are placed in parallel. As a result, the perpendicular arrangement of conductors leads to an increase in crosstalk at nodes *V*3 and *V*4. Thus, at $h = 0.2$ mm, the crosstalk in node *V*3 increased by 1.5 times, in node *V*4 – by 2 times, at $h = 2$ mm – by 1.2 and 1.4 times, respectively.

The voltage waveforms at nodes *V*5 and *V*6 are shown in Fig. 12 (a, b), and the relationship between the maximum crosstalk and *h* are illustrated in Fig. 14 (c, d).

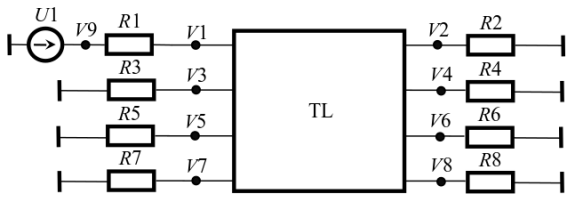

Fig. 10. Schematic diagram of the ESD impact on the TL

Fig. 12(a) shows that the waveform and crosstalk amplitude at nodes *V*5 and *V*6 with perpendicularly located conductors coincide. In this case, the maximum amplitude does not exceed 15.7 V at $h = 1.6$ mm. With parallel conductors at the near end, the crosstalk is greater by 8.8 times, and at the far end – by 6.6 times (Fig. 12 (b)).

It is clear from the dependencies (Fig. 12 (c)) that an increase in h between perpendicularly located conductors from 0.2 to 2 mm leads to a decrease in the maximum amplitude by 2.4 times. With parallel conductors, an increase in h leads to a 2-times decrease in the maximum crosstalk at the near end and a 1.8-times increase at the far end (Fig. 12 (d)). The perpendicular arrangement of the conductors made it possible to maximally reduce the crosstalk at the near end by 9.3 times and at the far end by 6.6 times.

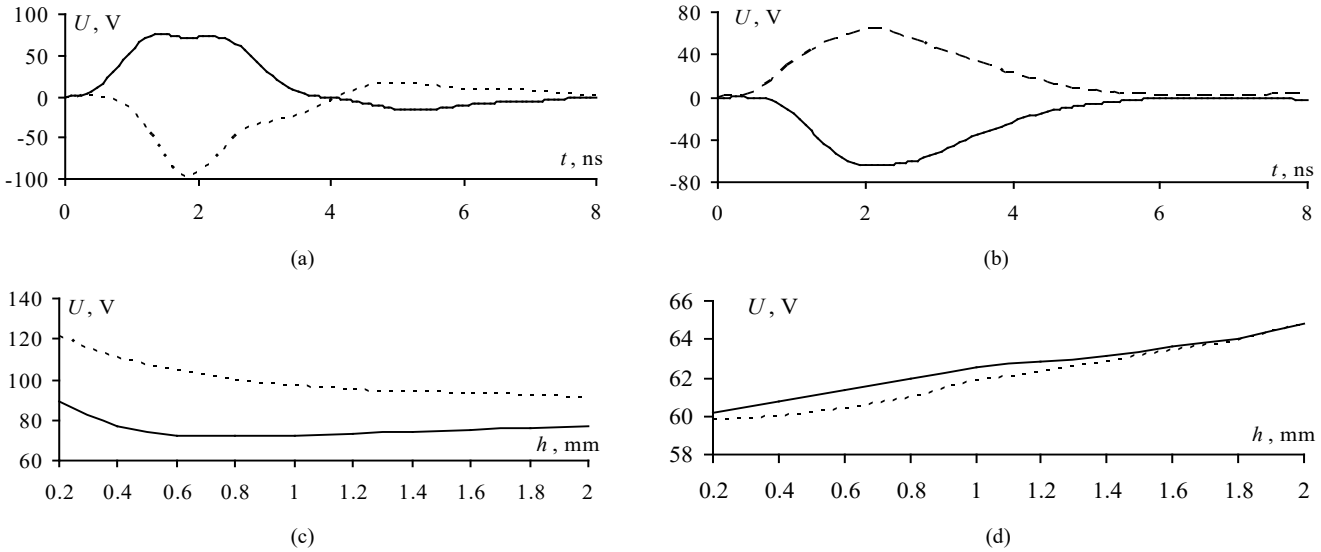

Fig. 11. Voltage waveforms at nodes *V*3 (—) and *V*4 (- -) and relationship between the amplitude and h under the ESD impact on the CTL with perpendicular (a, c) and parallel (b, d) conductor arrangement

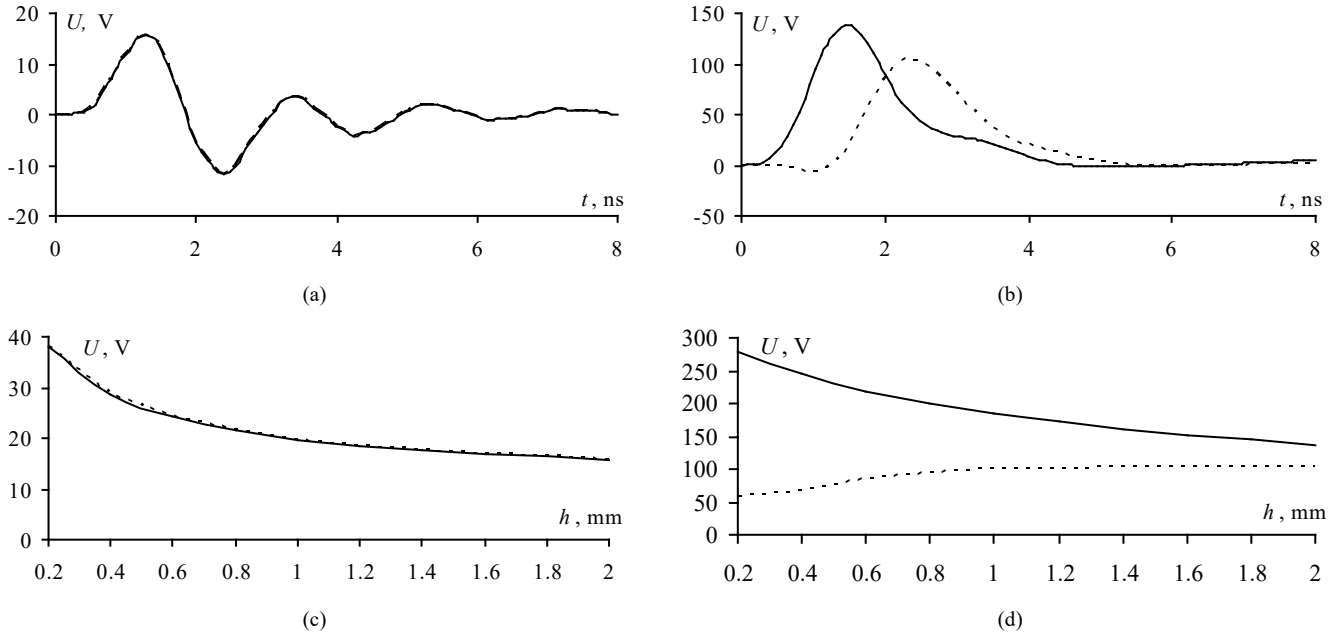

Fig. 12. Voltage waveforms at nodes *V*5 (—) and *V*6 (- -) and relationship between the amplitude and h under the ESD impact on the CTL with perpendicular (a, c) and parallel (b, d) conductor arrangement

The waveform and amplitude of voltages at nodes *V*7 and *V*8 with perpendicularly arranged conductors coincide with the waveform and amplitude at nodes *V*5 and *V*6 (Fig. 12 (a)). The waveform and amplitude of voltages at nodes *V*7 and *V*8 with parallel arrangement conductors coincide with the waveform and amplitude at nodes *V*3 and *V*4 (Fig. 11(b)), and the maximum amplitude does not exceed 70 V.

V. Conclusion

As a result, models of fragments of a two-layer PCB based on MTL, CTL and CopTL have been created. The capacitances between perpendicularly and parallelly located conductors on different layers of the PCB were calculated when the distance between them changes. It is shown that when the thickness of the glass-fiber laminate substrate increases by 10 times, the capacitance decreases by 2 times with perpendicular conductor arrangement and by 7.4 times with parallel arrangement. At the same time, the capacitance for perpendicularly arranged conductors is 10.3 times less at $h = 0.2$ mm and 2.8 times less at $h = 2$ mm than with their parallel arrangement. It is shown that for PCB fragments based on the CTL, the increase in h leads to a decrease in the self and an increase in the mutual capacitance. The self-capacitance is 6.2 times larger, and the mutual capacitance is 3.4 times smaller with parallel arrangement of conductors in comparison with perpendicular one. It is shown that increasing h leads to a decrease in C for perpendicularly arranged coplanar waveguides and an increase for parallelly arranged coplanar waveguides. The mutual capacitance decreases in both cases. Thus, with parallel arrangement and $h = 0.2$ mm the value of C_c is 13.2 times greater, and at $h = 2$ mm – is 4.7 times. Increasing the distance between active and passive conductors leads to a decrease in their self and increase in mutual capacitances.

The analysis of the influence of conductor arrangement on the crosstalk when the PCB is exposed to ESD showed that for MTL-based models, the perpendicular arrangement of conductors leads to a decrease in the crosstalk at the near end by 8 times, and at the far end by 5.5 times. An increase in h between parallel conductors leads to a decrease in the crosstalk at the near end and an increase at the far end. The perpendicular conductor arrangement of the CopTL reduced the crosstalk at the near end by 35 times, and at the far end up to 8 times. When analyzing the CTL-based PCB fragments, it is noticed that the perpendicular arrangement of conductors leads to an increase in the crosstalk on the passive conductor located on the same layer as the active one by a factor of 1.5. However, the crosstalk on conductors located on the opposite layer was significantly reduced at the near end by a factor of 9.3 and at the far end by a factor of 6.6.

Thus, when designing REE, it is necessary to take into account these features of the conductor arrangement, and the developed models can be used to comprehensively analyze electronic components of REE under the destabilizing influence of ESD.

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