SIGNAL INTEGRITY ANALYSIS
FOR THE FOUR-LAYER REFLECTION SYMMETRIC MODAL FILTER

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Abstract. The article presents the results of signal integrity analysis for a four-layer reflection symmetric modal filter and determines a potential field of application for such devices. The authors performed a simulation and experimental study in the range from 0 to 1.5 GHz. The results show that the average level of insertion loss in the passband does not exceed -18 dB, which demonstrates good agreement. The insertion loss does not significantly attenuate the useful signal. After the modal filter was defined in the frequency domain, the authors used the Advanced Design System to analyze the time characteristics. Pseudorandom binary sequences with bitrates from 0.125 to 0.5 Gb/s were excited to the input of the device in the Advanced Design System. The eye diagrams show that the modal filter has an excellent performance in terms of signal integrity. Thus, at the fastest data rate, the jitter does not exceed 39.5 ps. The maximum value of amplitude noise was 71 mV. It is possible to achieve significantly lower values of jitter and amplitude noise for the modal filter using its optimal geometric and electrical parameters. The results of the electrodynamic simulation are in good agreement with the experimental results.

Keywords: signal integrity, reflection symmetric modal filter, electromagnetic compatibility, pseudorandom binary sequence, eye diagram.

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Introduction

The design problems of printed circuit boards (PCBs) and high-frequency electronics assemblies are becoming increasingly relevant [1]. The requirements for the integrity of the power supply systems and the useful signal are increasing every year. One of the most important tasks in electromagnetic compatibility (EMC) is to ensure noise immunity of radioelectronic equipment (REE) [2, 3].

To provide EMC of interconnections, the technology of modal filtering and structures based on it, namely, modal filters (MF), were proposed in [4]. In contrast to the widely used microstrip transmission lines and coplanar waveguides with low interference immunity, MFs can protect REE from ultra-wideband (UWB) interference. Such devices meet the requirements of the EMC standard in the field of protection against powerful UWB interference [5].

There are many configurations of MFs according to their functional purpose [6, 7]. The reflection symmetric MFs are interesting in that they allow the attenuation of the UWB interference received at any of the structure inputs with the same efficiency [8]. These MFs can connect four different nodes in both power distribution and data transmission systems. Fig.1 shows the location of the reflection symmetric MF in the electrical circuit and an example of its implementation in a PCB.

Depending on signal parameters and transmission line topology, earlier transmitted bit sequences can affect the fronts and amplitudes of subsequent pulses. This effect can be caused by interference of incident and reflected waves, crosstalk, symbolic dispersion, and different velocities of their propagation along the transmission line, which leads to deviations in phase and amplitude of the useful signal. Previously, the authors have conducted several studies of the noise immunity properties of the four-layer reflection symmetric MF in the frequency and time domains [9, 10]. However, signal integrity has not been considered. Meanwhile, such research is relevant as it will allow determining an application field for reflection symmetric MFs in data transmission systems. Therefore, the aim of this work is to analyze signal integrity in a four-layer reflection symmetric MF.
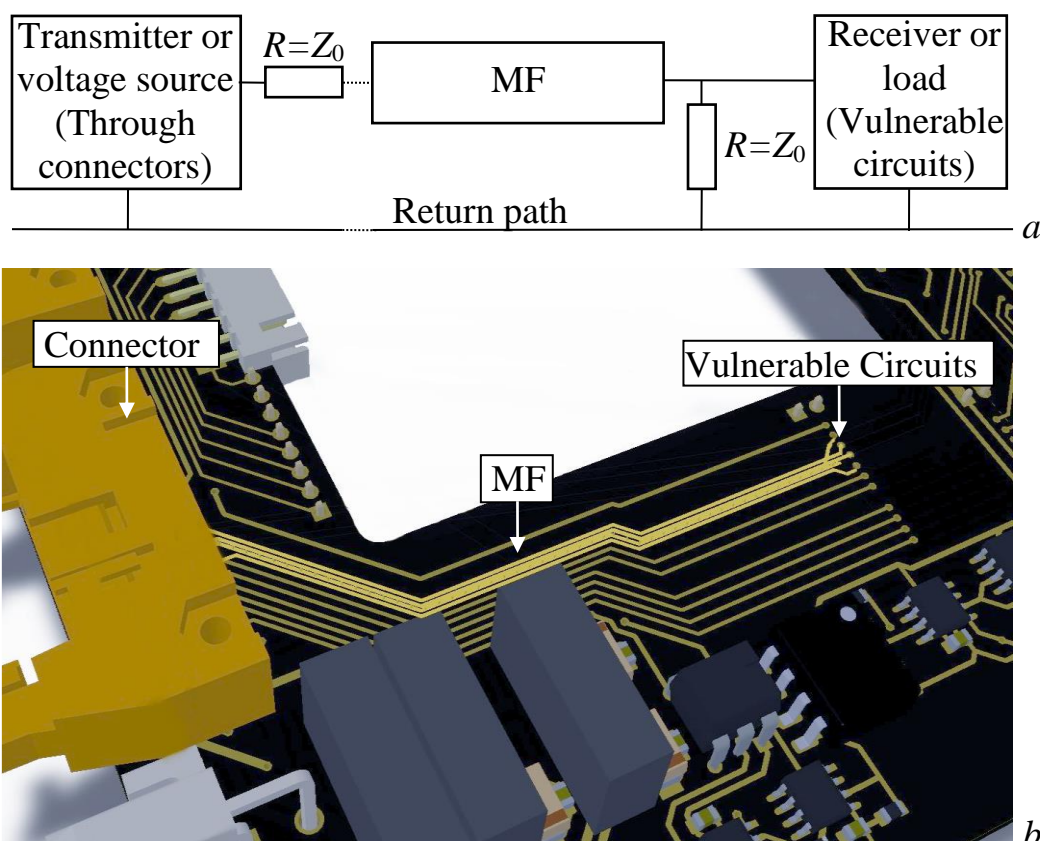
Fig.1. Location of the proposed MF in an electrical circuit and example of its implementation in a PCB

This paper is divided into three sections. Section I describes the device under study and the approaches used. Section II presents the results of the signal integrity analysis and compares them with well-known studies. Finally, a general conclusion is given in Section III.

1. Construction, Simulation and Experimental Techniques

This Section presents the cross-section and connection diagram of the four-layer reflection symmetric MF, the materials used, simulation methods, as well as the experimental techniques.

Fig.2 shows the cross-section and connection diagram of the MF, which is a four-layer PCB with four signal conductors and two return conductors. A useful signal source with resistance R_{source} is connected to Cond 1 at the near end, and a load with resistance R_{load} is connected to the far end. Resistors R are connected to conductors Cond 2 – Cond 4. To minimize reflections from the MF ends, all resistors were equal

to 50 Ω. Thus, the matching of the wave resistance of the structure with the measuring tract was achieved.
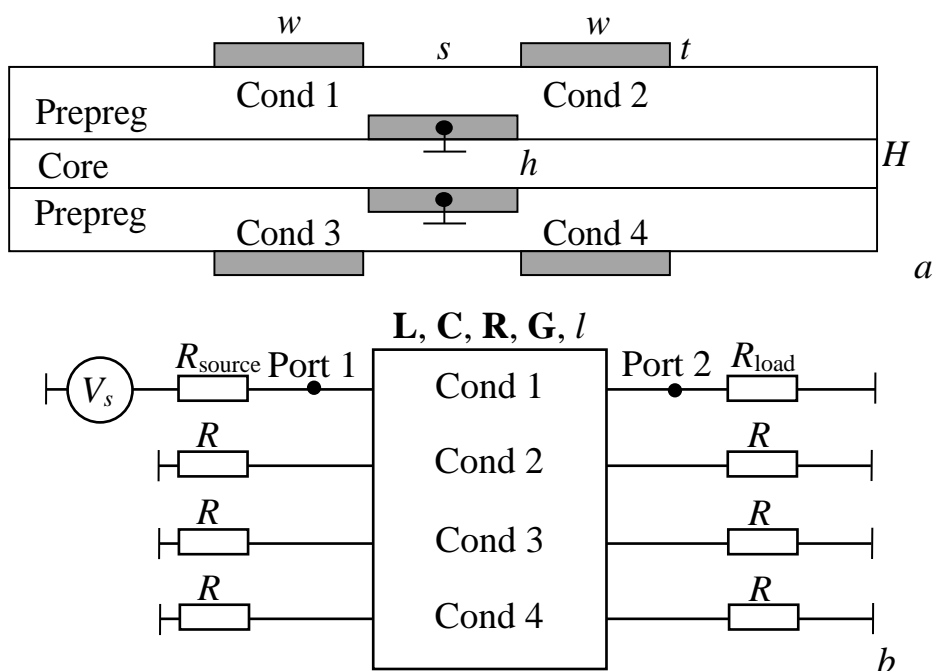

Fig.2. Cross-section (*a*) and connection diagram (*b*) of the reflection symmetric MF

The parameters of the MF cross section were the following: the conductor width w=1 mm, the conductor spacing s=0.7 mm, the conductor thickness t=0.035 mm, the core thickness h=0.51 mm, and the total PCB thickness H=1 mm. The electrical parameters of the core and prepreg (FR-4) were as follows: the relative permittivity ε_r=4.3, the tangent of dielectric losses tgδ=0.018. Parameters are given for frequency of 1 MHz. We should note that the investigated structure is only a fabricated prototype of the reflection symmetric MF from [10]. It makes it possible to evaluate the signal integrity on a normalized length of l=1m. In real PCBs, the length and total dimensions of such a MF can be much smaller. Miniaturization of MF parameters is achieved by optimizing its geometric parameters for a particular PCB.

The authors used a numerical method of analysis, in particular, the method of moments, implemented in the Advanced Design System 2020 (ADS). The Maxwell equations were solved without any simplifications. For the MF simulation, Gerber files of the top, bottom, and inner layers of the previously produced layout were imported into ADS (Fig.3). These files contain complete information about the two-dimensional geometry of the layout. The total dimensions of the layout were 340 by 31 mm.
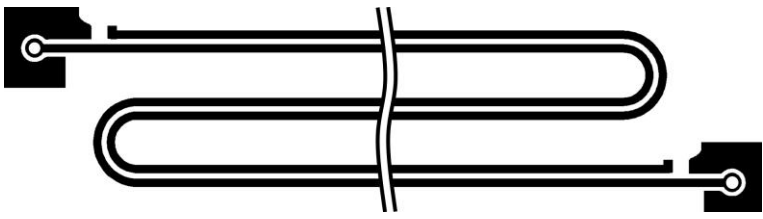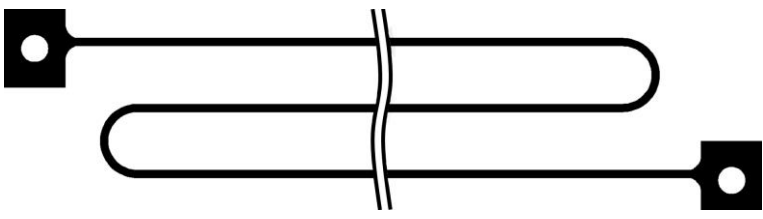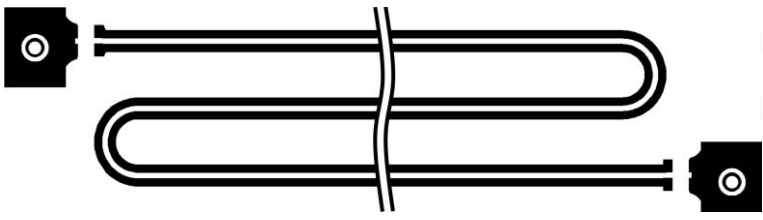
Layers	Layouts
Top	
Inner	
Bottom	

Fig.3. Layers of the MF under study

The authors simulated the MF in the frequency range from 0 to 1500 MHz. In the general case, the construction and calculation of the grid took place at the highest frequency of the study. The grid density was 20 cells per wavelength. To correctly account for edge effects, the conductor edges were additionally divided into segments, the sizes of which were automatically determined by the simulation software. To account the frequency dependence of the core and prepregs, the mathematical model of Svensson/Djordjevic losses was used [11, 12]. Copper with a conductivity of 59.6 MS/m was used as the conductor material.

To determine the information-dependent deviations of the phase and amplitude of the signal passing through the MF, it is required to analyze a large number of bit sequences. In this study, a pseudorandom bit sequence (PRBS) of 10,000 bytes was used. Specifically, we employed three PRBSs with different parameters. Fig.4 shows their location, and Table 1 presents their parameters.
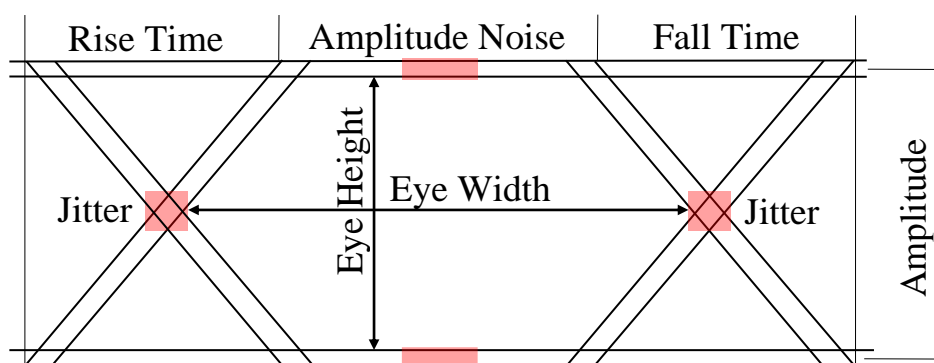
Fig.4. Location of the PRBS parameters

Table 1. PRBS Parameters

№	BitRate (Gb/s)	Period (ns)	Rise/Fall Time (ns)	Amplitude (mV)
1	0.125	8	0.8	
2	0.25	4	0.4	1000
3	0.5	2	0.2	

Fig.5 presents the experimental setup used to determine the MF in the frequency domain. The device under study was connected to a vector network analyzer (VNA) ZVA 40 using high-frequency cables. Before the measurement, we performed a two-port SOLT calibration in the frequency range from 10 to 1500 MHz.
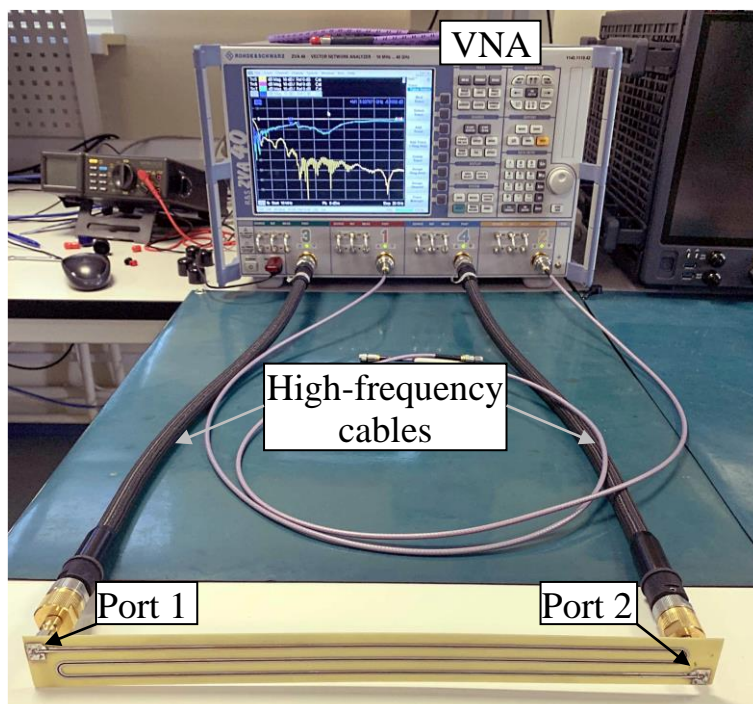

Fig.5. Measurement setup to analyze MF frequency characteristics

After the MF was defined in the frequency domain, authors used ADS to redefine it in the time domain. For this purpose, the measured *S*-parameters were uploaded to the ADS, and the PRBSs were analyzed. Fig.6 shows a scheme for analyzing the MF characteristics in the time domain in the ADS.
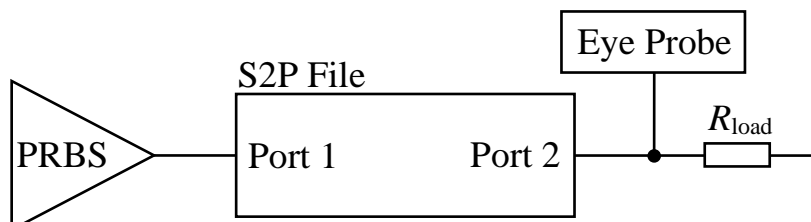

Fig.6. Scheme for analyzing MF characteristics in the time domain in the ADS.

2. Signal Integrity Analysis

This section presents the results of the signal integrity analysis in the frequency and time domains.

Fig.7*a* presents the frequency dependence of the reflection coefficients $|S_{11}|$ obtained from the simulation and measurement. We can see that $|S_{11}|$ values do not exceed -10 dB in the whole investigated frequency range. There are discrepancies between the results of the simulation and measurement. First, this may be explained by the unaccounted influence of coaxial-microstrip transitions. The $|S_{11}|$ values obtained from the simulation show better agreement of the MF. Fig.7 shows the frequency dependence of the reflection coefficients $|S_{21}|$ obtained from the simulation and measurement.

Fig. 7 shows that the investigated MF is a low-pass filter. The cutoff frequencies (determined by the -3 dB level) were 250 and 270 MHz for measurement and simulation, respectively. Both dependencies agree well. The deviation of the measurement results from the simulation, in this case, could be explained by the difference between the real electrical and geometrical parameters of the layout and the numerical model.

In terms of signal integrity, in the MF bandwidth, the level of return loss does not exceed 10 dB. Their average values obtained in measurement do not exceed -18 dB. In the insertion loss analysis, the characteristic decreases monotonically right up to the

first resonance frequency. The phase-frequency characteristics obtained in measurement and simulation agree well. Almost complete coincidence is achieved in the passband. According to the results obtained, it can be assumed that insertion loss will not distort the useful signal much.
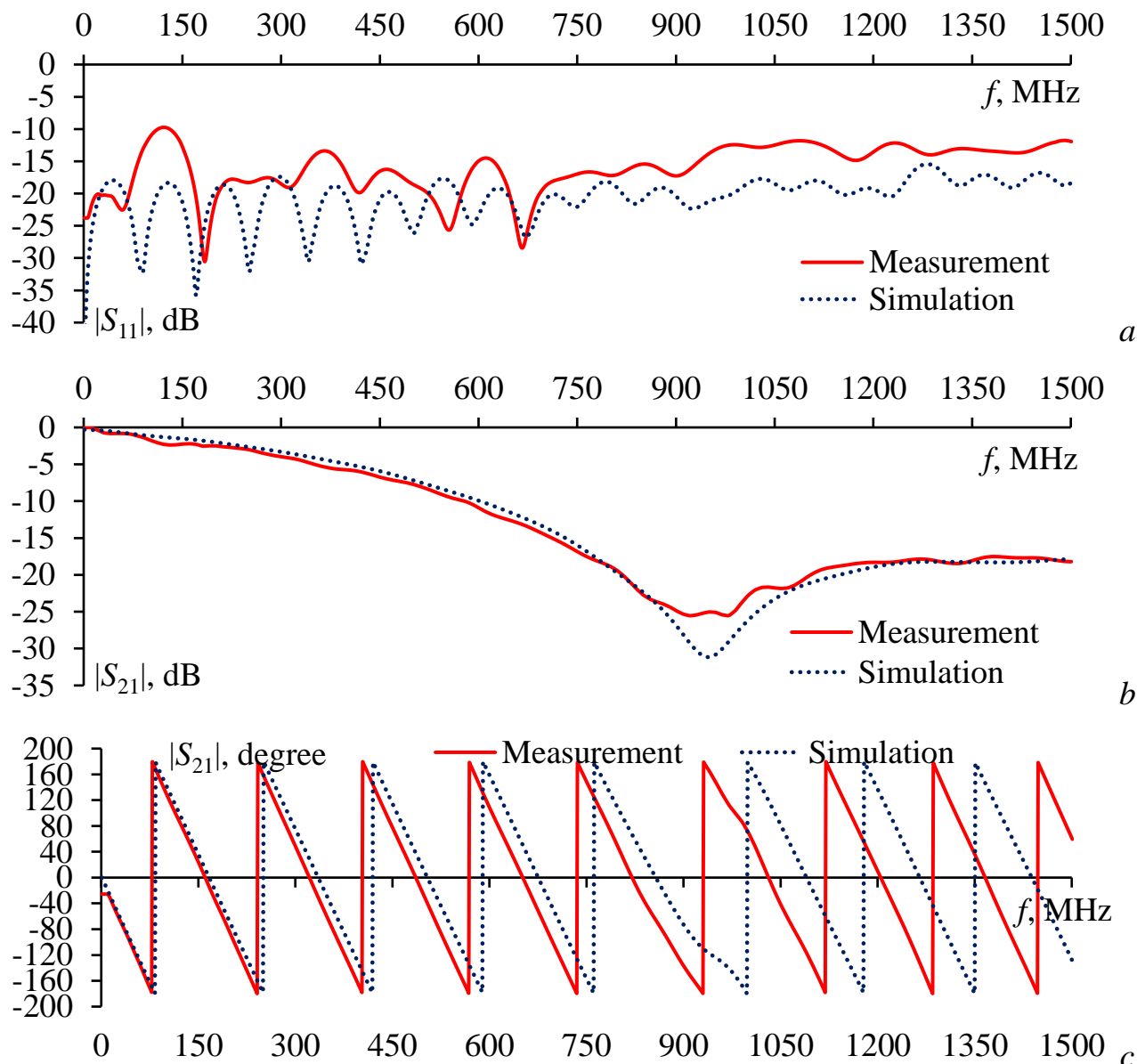

Fig.7. Frequency dependence of $|S_{11}|$ (a) and $|S_{21}|$ (insertion loss (b) and phase (c))

Fig.9 presents the eye diagrams for the three PRBSs obtained during the measurement. The contour inside the diagrams also represents the results obtained during the simulation.

We can see that at all examined data rates, the "eye" remains open. The smallest distortions are observed at the lowest bit rate. The highest distortions are observed at 0.5 Gb/s, which lies outside the bandwidth. We can see that the simulation results are

in good agreement with the experiment. However, minor differences in this case can be caused by the fact that, besides the data-dependent jitter, there are other components of jitter in the measurement. The internal jitter of the experimental setup, as well as random jitter, may have a significant influence.
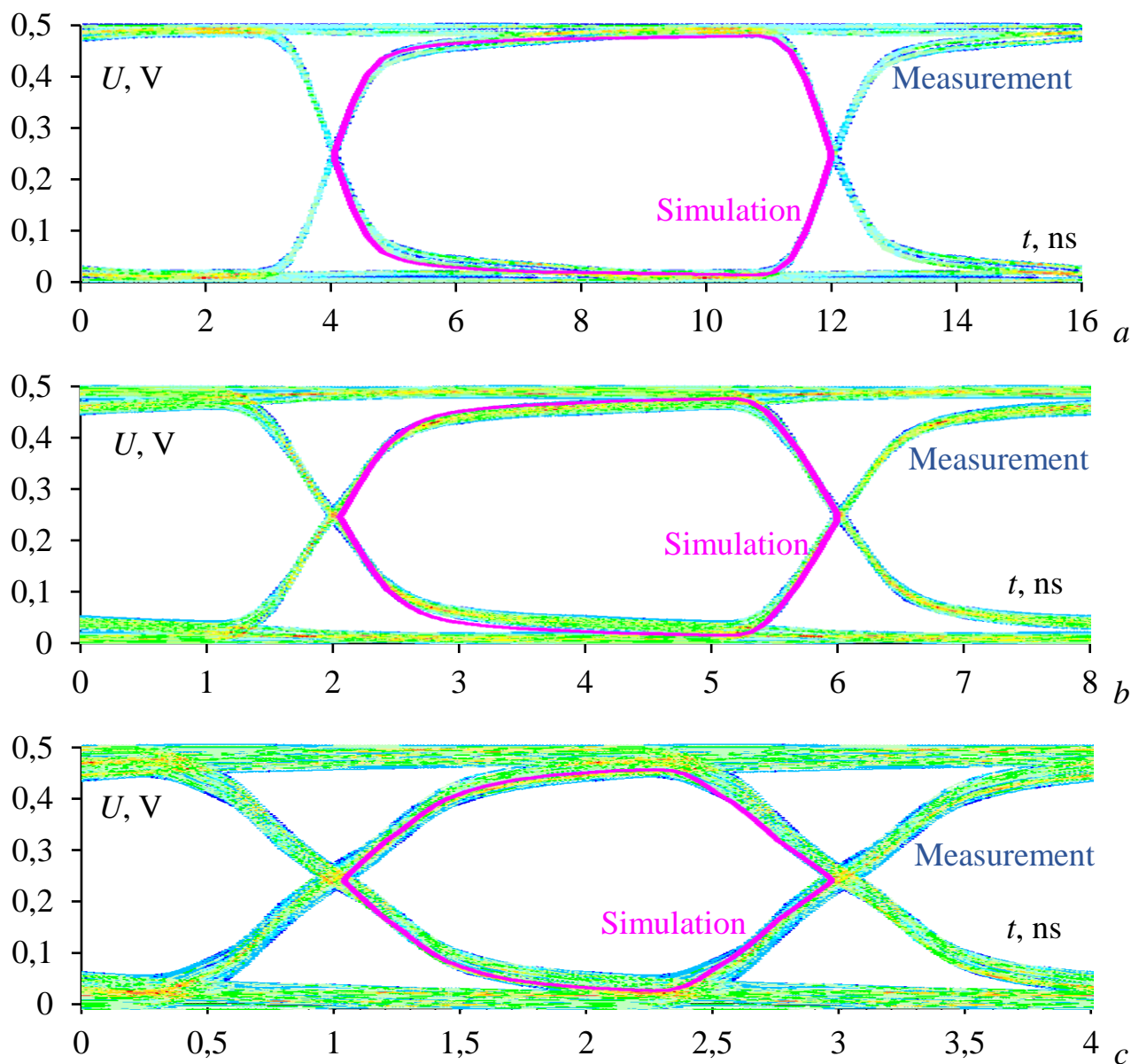

Fig.8. Eye diagrams for the MF: 0.125 (*a*), 0.25 (*b*), and 0.5 (*c*) Gb/s

Table 2 presents the results of simulating and measuring signal integrity in the time domain. We can see that, as the bit rate increases, the quality of the useful signal decreases. Thus, in the case of the measured values, the root mean square (RMS) of jitter increases with increasing the bit rate. The amplitude noise also increases from 30 mV at 0.125 Gb/s to 71 mV at 0.5 Gb/s.

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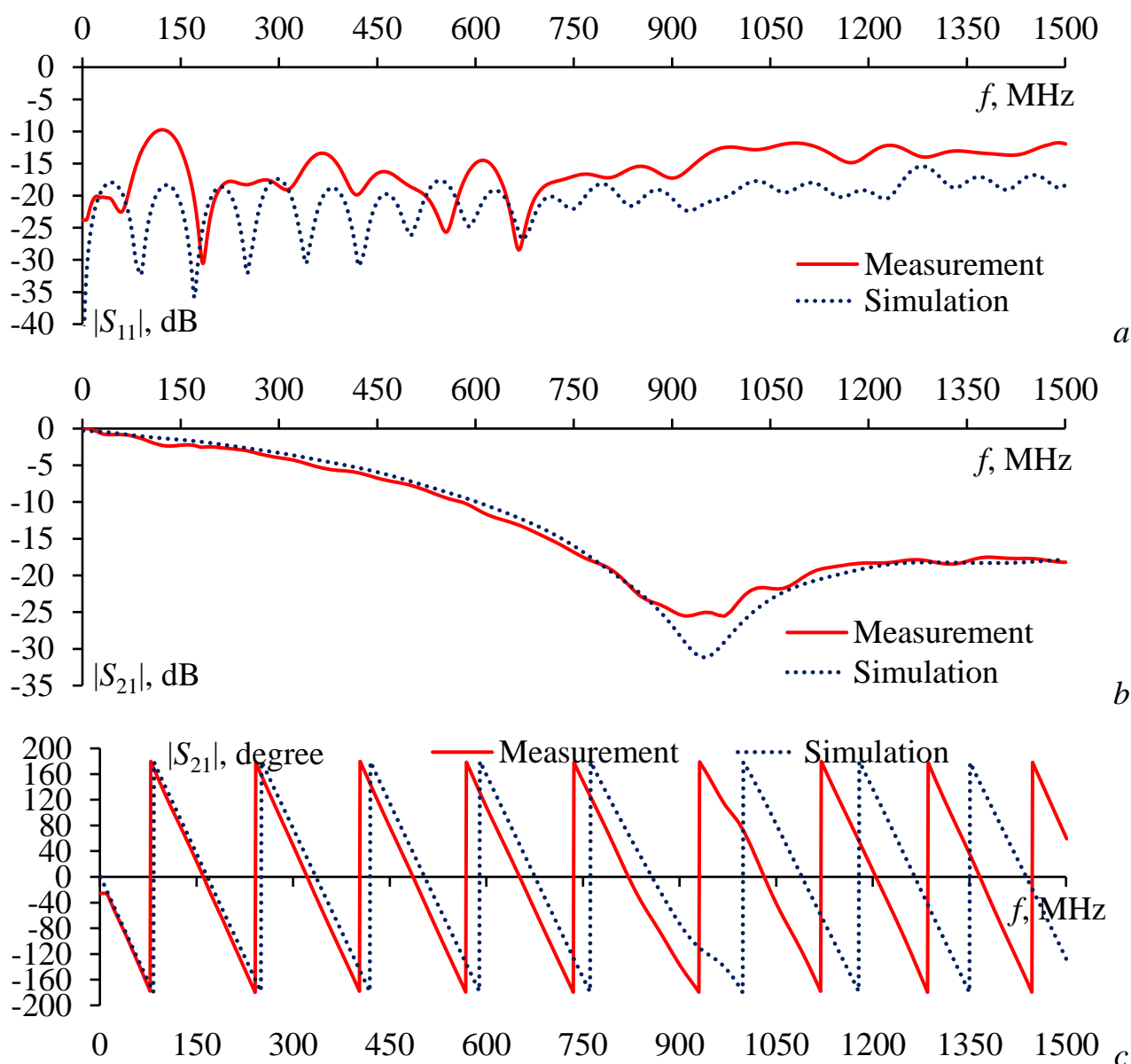
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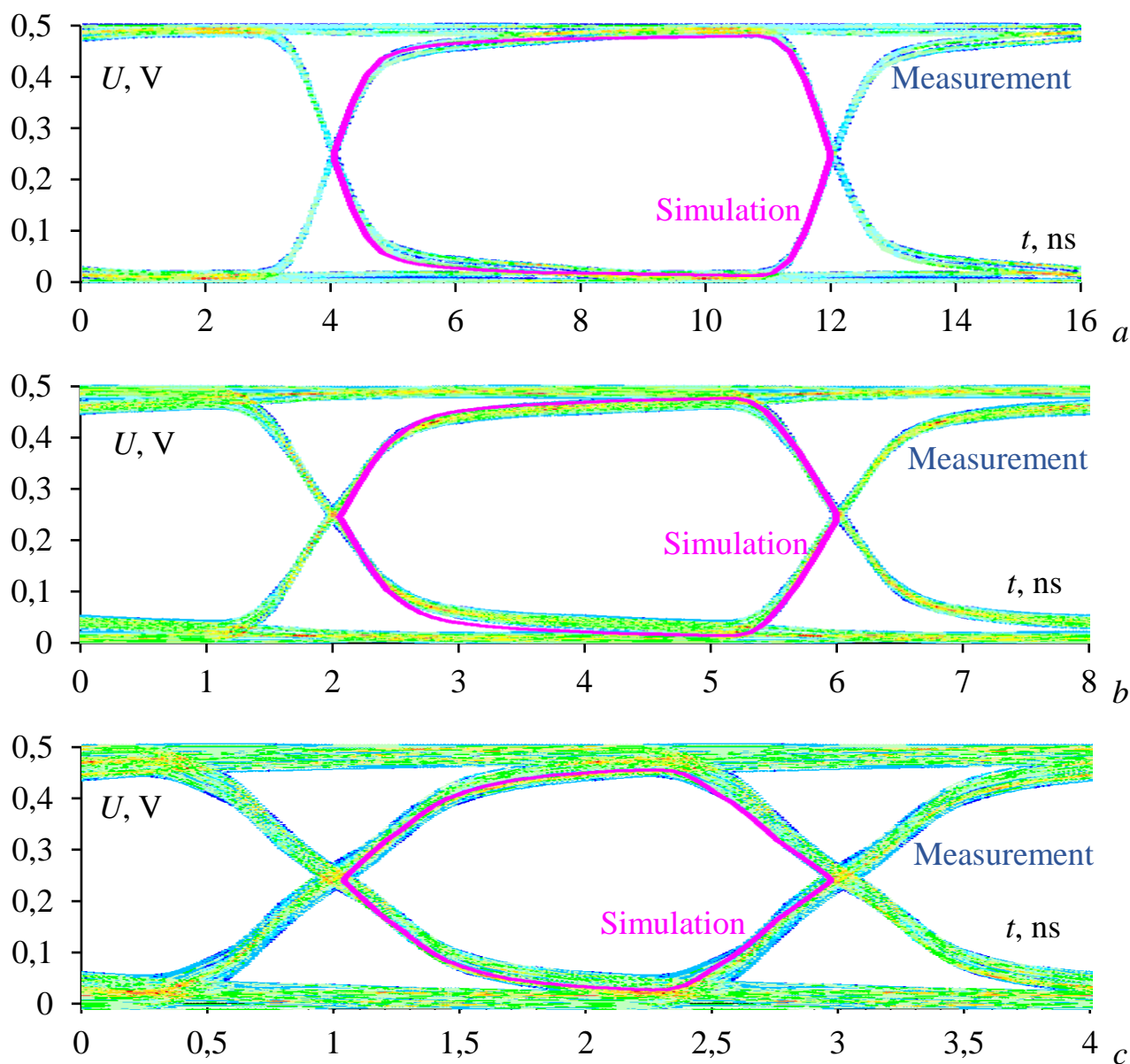
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The results show good signal integrity for the MF in the bandwidth. At low data rates, the insertion and return losses have minor effect on the useful signal waveform. However, as the frequency increases, losses and modal distortions have more influence. Thus, at a bitrate of 0.5 Gb/s, the front of the signal decomposes and a further increase in speed can lead to even greater distortions. In this case, the "eye" will be closed, and

the reception of a useful signal will be impossible. Meanwhile, even at 0.5 Gb/s, the studied MF shows good signal quality characteristics. The average level of insertion loss in the range from 0 to 500 MHz does not exceed -17 dB. In terms of insertion loss from the eye diagrams, the signal amplitude decreased. In most applications, the demonstrated signal integrity level is typical [13–16]. Thus, for example, in microstrip transmission lines on dielectric with small tgδ, the jitter of 90 ps was obtained at the length that is many times less than the length of the investigated MF [17]. In addition, modern data transmission systems use data coding, which increases noise immunity. To achieve lower jitter and amplitude noise, it is reasonable to reduce the MF length and use a dielectric with a lower tgδ.

Table 2. Eye Diagram Parameters

№	*Jitter RMS (ps)*	*Eye Width (ns)*	*Eye Height (mV)*	*Amplitude Noise (mV)*
1 (Measurement)	21.5	7.92	0.419	30
1 (Simulation)	< 1	> 7.99	0.464	8
2 (Measurement)	27.9	3.92	0.374	58
2 (Simulation)	14.5	3.96	0.437	18
3 (Measurement)	39.5	1.83	0.325	71
3 (Simulation)	18	1.95	0.394	33

Conclusion

Thus, the paper presents the results of signal integrity analysis for the reflection symmetric MF in the frequency and time domains. With the use of the VNA, the authors defined the investigated device in the frequency domain. ADS was used to redefine it in the time domain. The results show that the MF has good signal integrity performance. When building the MF with optimal geometrical and electrical parameters, it is possible to achieve significantly lower values of jitter and amplitude noise. At the same time, the results of the electrodynamic simulation are in good agreement with the experimental results.

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