Method for Synchronizing a Group of Heterogeneous Microcontrollers with Time Control of Synchronous Work

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Abstract— A method to synchronize a group of microcontrollers with different clock frequencies of their own generator is proposed. The algorithm of each microcontroller operation in the group and the block diagram of the group consisting of N microcontrollers are presented. Timing diagrams of signals of synchronous operation and clock pulses of the microcontrollers group are given. The result of the work, at the first stage, is the counting of received clock pulses by microcontroller software, which allows synchronizing the microcontrollers performing a task using the different system frequencies. In the second stage, the use of a precision real-time clock and of an «AND» gate ensures high synchronization accuracy at the time of the start and end of the work. A program that calculates the number of clock pulses for each microcontroller of the synchronized group based on the clock frequency of the microcontroller, on the frequency of the clock generator and on the period of synchronous operation is developed. The calculated coefficients can be used in the development of the microcontroller synchronization code. Using hardware and software and two synchronization stages, it became possible to obtain high accuracy and flexibility in setting the synchronous operation of a group of heterogeneous microcontrollers.

Keywords— synchronization, microcontroller, heterogeneous computer network

I. INTRODUCTION

Microcontrollers (μC) are widely used inside radioelectronic equipment. This was facilitated by a large variety of the model series of computing architectures (8-32 bit), characteristics of computing and peripheral devices, communication interfaces (I²C, 1-Wire, SpaceWire, RS-232, RS-485, CAN, USB and etc.). The use of at least two μ Cs expands the functionality and increases the computing power of a radioelectronics equipment, and also allows to work with a large number of peripheral devices. An increase in the number of tasks assigned to a radioelectronic equipment, for example, when controlling a large number of spaced devices, designing data acquisition systems from sensors, etc., requires the synchronization of a group of μ Cs, each of which performs a particular task. Therefore, there is a need for a group of μ Cs to perform actions with a certain periodicity, in connection Maxim P. Sukhorukov, Yuriy A. Shinyakov Scientific Research Institute of Space Technologies Tomsk State University of Control Systems and Radioelectronics, TUSUR Tomsk, Russia

with which the problem of synchronizing their work arises. Synchronization is necessary when performing tasks in real time [1]. Well-known methods for synchronizing µCs involve the use of precision quartz oscillators. There are methods of time synchronization using non-precision CMOS generators [2]. The synchronization problem is quite extensive [3], because clock generators, used in distributed locations are not absolutely accurate and do not support real-time accuracy [4]. One of the known synchronization methods is the use of a common external clock generator (ECG) for each μ C in a group. This method is actively used [5, 6], however, it has many disadvantages such as: μC group should be of the same type; the work of the μC group is possible only on one frequency; an increase in the number of μ Cs greater than four leads to unstable operation of the μC due to the clock waveform distortion due to the difficulty of maintaining the signal integrity. The deficiency of control of synchronous operation and means of regulation of the period of synchronous operation of the μ Cs group also causes limitations on the possibility of using the existing synchronization methods. Methods for synchronizing the work of the µCs group of different manufacturers, at different system frequencies, are not known to the authors. Thus, it is useful to perform an analysis of the software and hardware of the μ C and to develop a method that eliminates the above disadvantages. The purpose of the work is to develop a software-hardware method for synchronizing the operation of two or more µCs with the ability to control the period of synchronous operation.

II. PRINCIPLE OF THE PROPOSED METHOD

A method for synchronization of the μ C group is proposed, which allows to agree on the performance of a common task by a group of μ Cs that are not connected by an interface. μ Cs of synchronized group are not divided into "master" and "slave" (Master-to-Slave). At the same time, each μ C performs its own instructions (code), without affecting the work of other μ C groups. The block diagram of the device that implements the method of synchronizing the μ C group is shown in Fig. 1.

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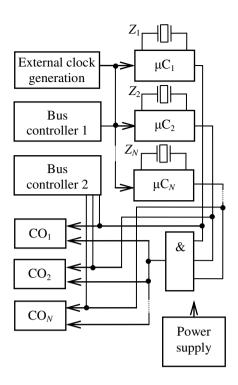


Fig. 1. The block diagram of the device synchronizing the μ C group

The synchronization device allows to synchronize the operation of μ Cs from different manufacturers and perform flexible synchronization settings. Synchronization of μ Cs is carried out with minimal changes in the circuit of radio electronic devices. The result is achieved due to the use of each μ C own (internal/external) clock, the counting each μ C clock from an external clock, the setting the μ C timers/counters, the confirmation signal (of the μ Cs group synchronization) through the AND gate.

The circuit (Fig. 1) operation principle is as follows. At the output of the external clock generator, the sheduled frequency (f_{ECG}) of clock pulses is set, which are applied to one of the digital inputs of the port of each μ C in a group of $N \mu$ Cs. The μ C input must support an external interrupt. The *N*-th μ C operates at the desired $f_{\mu CN}$, frequency corresponding to the clock pulses generated by the internal or external clock from the internal or external (Z_N) crystal. The frequency f_{ECG} is given by the condition $f_{ECG} < f_{uCN}$, otherwise it will be impossible to calculate the number of clock pulses from an external clock (Fig. 2).

When an external interrupt is triggered by the μC , a function corresponding to this interrupt is called, which increments the counter variable in the memory of the μC . Thus, the received clock is counted from the external clock by each μC in the group.

As soon as the counter variable in the memory of the μ C, responsible for the counting of the synchronous pulses (Fig. 3), reaches a certain value, an internal interrupt is triggered ($S_{\mu C1} - S_{\mu C4}$), responsible for the start of synchronous operation.

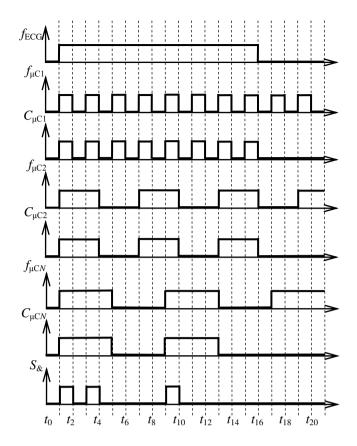


Fig. 2. Calculation of the number of sync pulses by a group of μ Cs

The S_{SCK} event at time t_3 (Fig. 3) means that all μ Cs are ready for synchronous operation. In this case, the following commands are successively executed: resetting the sync counter and starting the synchronous operation counter of the μ C group with the time interval from t_3 to t_9 (Fig. 3). The synchronous operation counter can be implemented by the μ C hardware timer, or programmatically in the μ C's memory. The synchronous interval is calculated based on the $f_{\mu C}$, f_{ECG} and the specified period of synchronous operation.

At the time of t_9 , when at least one μ C from the group completes its operation, the synchronous operation ends (the desynchronization of a group of μ Cs). The following commands are executed: exit from the function of synchronous operation of a group of μ Cs; reset the synchronous period counter value; transition to the calculation of sync pulses. Fig. 3 shows, that the $S_{\mu C1}$ and $S_{\mu C3}$ completed the work at the same time, while the other μ Cs still continued to work. However, this result is no longer taken into account, since there is no signal from the AND gate.

All μ Cs can work on different frequencies and the synchronization count is calculated by everyone. Therefore, the onset of synchronous operation of each μ C may differ by the period of time t_S between the readiness of the first and last μ C in the group. It can be calculated as

$$t_S = |t_O - t_E| \tag{1}$$

where t_0 – the start time of synchronous operation of $S_{\mu C(2N+1)}$; t_E – the start time for synchronous operation of the $S_{\mu C(2N)}$. Reducing the time interval Δt to $t_N - t_{N-1}$ results in an improved synchronization of the μ C group.

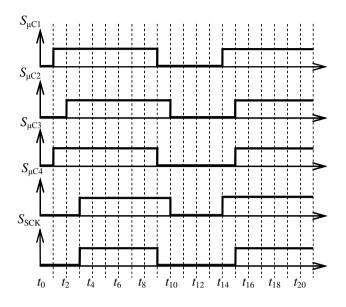


Fig. 3. Timing diagram of signals of synchronous operation of a gr. of µCs

III. PROGRAM PART

To calculate Δt , the software «Synchronizer for the operation of a group of μ Cs» was developed, which allows simulating the synchronous operation of a group of μ Cs (Fig. 4) [7]. The functions of the simulator are divided into two blocks. The first block calculates the number of sync pulses for each μ C (Tabl. 1). In the second, a simulation of the work of a group of μ Cs occurs.

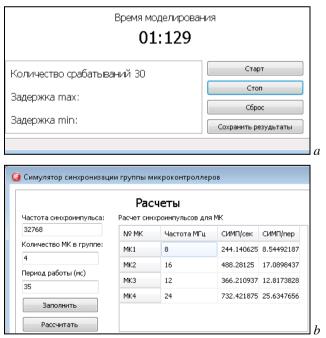


Fig. 4. Synchronization simulator (*a*) and a block for calculating the coefficients (*b*) for the synchronous operation of a group of μ Cs

Simulation allows to verify and optimize the algorithm without the need to develop the program code of the μC and shorten the time to develop a prototype device.

TABLE I. CALCULATIONS OF THE SIMULATOR PROGRAM

μC	Frequency (MHz)	SIMP/s	SIMP/per
1	8	244.141	85.4492
2	12	366.211	128.174
3	16	488.281	170.898
4	24	732.422	256.348

As the initial data, the duration (ms) of the synchronous operation, the clock frequency and the number of μ Cs of the group are entered. Calculation of the optimum number of sync pulses (SIMP/s) for each μ C is based on the frequency of the external clock and the μ C. The calculated number of sync pulses for the specified synchronous operation period (SIMP/per) is used by the μ C counter to determine the beginning of the common operation by calling the internal interrupt by raising the "start" flag in the μ C code. Running the simulator allows you to check the calculated values. Thus, the duration of synchronous operation of a group of μ Cs is monitored, performing a common task. The algorithm for operation of each μ C in a group is developed (Fig 5).

Based on the results of the simulation, for each μ C the following data is recorded: the number of received clock signals; time of beginning and end of the general operation; the time interval between the first and last μ C that started synchronous operation; the number of synchronous operations. Based on the data received in the simulator, a file with records of events with all information for the simulation period is formed. The received data can be saved on a computer to a file with the extension *.txt. To do this, the function «save results» is provided, which allows to analyze the results of the calculation in order to optimize the synchronizing the work of μ Cs group.

However, the simulator is limited in capabilities and can not perform the job with an accuracy comparable to the μ C. The computer and μ C commands differ in architecture and calculating capacity. It is impossible to provide all the factors of the code work in the μ C. In addition to the synchronization algorithm code, there may be other tasks in the μ C that affect the operation of the μ C. Therefore, you can effectively manage the resources of the μ C using real-time operating systems. In this case, the μ C's tasks are managed by the scheduler (task manager), whose main task is to allocate equal time intervals and resources of the μ C for the task in accordance with its priority.

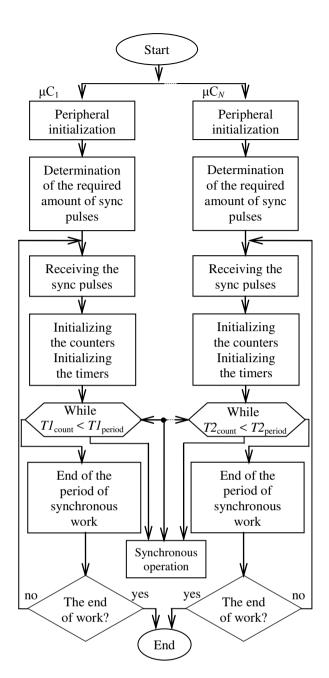


Fig. 5. The algorithm of operation of each μC in a group

IV. CONCLUSION

A hardware-software method for synchronizing the operation of a group of μ Cs is developed. It allows you to perform a task by a group of μ Cs, using minimal means. This method can be applied to ready-made devices in the form of a separate module, or by modifying the scheme of the final device. The versatility of the method lies in the fact that it allowes to synchronize the operation of μ Cs from different manufacturers. It is also possible to obtain a flexible synchronous operation period. The developed «Simulator of synchronous operation of a group of μ Cs» allows calculating the values of the timer coefficients of the counters of μ Cs and also check the calculated values by running the simulator, which allows to implement a certain mode (algorithm) for synchronizing a group of μ Cs.

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