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Simulating Integrated Circuit Immunity to Powerful Conducted Emissions in Circuits with Single Modal Reservation

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***Abstract*— The paper considers the model of IC immunity to powerful conducted interference in circuits with a single modal reservation. The model is analyzed under the influence of pulses of the same and different polarities with and without IC power supply. The results show that the surge protection system based on dual diodes without power supply protects better against bipolar pulses. The efficiency of such a protection system strongly depends on the parasitic parameters. When the upper boundary frequency of unwanted signals increases the efficiency of protection decreases. At the same time, the combined application of such a system with passive protection devices based on modal filtration allows for a desirable level of attenuation of conducted interference even in the presence of unwanted parasitic parameters.**

***Keywords*— integrated circuits, ultra-short pulse, electromagnetic compatibility, modal reservation, schematic simulation.**

I. INTRODUCTION

During the operation of high-voltage and high-frequency equipment, there are complex transients that can generate broadband electromagnetic interference (EMI) [1]. A dangerous type of such interference is conductive EMI, in particular, ultra-short pulses (USP) [2]. They can damage radio-electronic equipment and bypass traditional interference protection systems (because these systems have limited performance). Such approach as reservation, or redundancy, is used to improve the reliability and fault tolerance of critical radio-electronic equipment (REE). Modal reservation (MR, or modal redundancy) is a type of cold standby [3]–[5]. Its main idea is to design a special layout of reserved (or primary) and reserving (or secondary) circuits to ensure strong electromagnetic coupling between them. Fig. 1 shows a connection diagram of a generalized transmission line and a cross-section of a microstrip line (MSL) with a single MR. Due to different propagation velocities of the USP, it is decomposed to a sequence of lower amplitude pulses [6].

In the case of a single MR, two unipolar pulses are obtained at the far end of the reserved conductor, and two bipolar pulses are obtained at the far end of the reserving conductor. Thus, with a sufficiently large amplitude and short duration of a USP, the components terminating not only the reserved (*R*3) but also the reserving (*R*4) transmission line may be at risk. Paper [7] presents the results of calculating *N*-norms at the far end of the reserved and reserving conductors of a device with a single MR. The N-norms of the decomposed pulses are analyzed there. The results showed that the probability of failure of the reserving circuit is lower than that of the reserved circuit. However, these results give a limited evaluation because they do not take into account a circuit design. To protect high-speed integrated circuits (ICs) against overvoltages and electrostatic discharge (ESD), semiconductor components, and diodes in particular, are most commonly used. Thus, for example, in [8] the authors investigated a novel gate-coupled silicon-controlled rectifier to effectively protect deep-submicron MOS circuits. The paper [9] presented a new high voltage swing bipolar ESD protection device which provides low leakage precision mixed-signal ICs operating at high voltages and high temperatures. Another study provided a novel power-rail ESD clamp circuit with a small time constant to achieve a longer turn-on time [10]. In [11], the authors demonstrated a PNP-based bidirectional ESD protection device with the base bias controlled by two pMOS transistors. The paper [12] proposed a novel RC-triggered bidirectional ESD protection circuit in SOI technology. In [13], the authors presented the analysis of a device failure caused by the on-chip ESD structure defects. To protect ICs from ESD and overvoltage, additional electronic components are also used - resistors, Zener diodes, TVS diodes, suppressors, and buffer microchips. For our study, we chose the circuit model from [14] because it

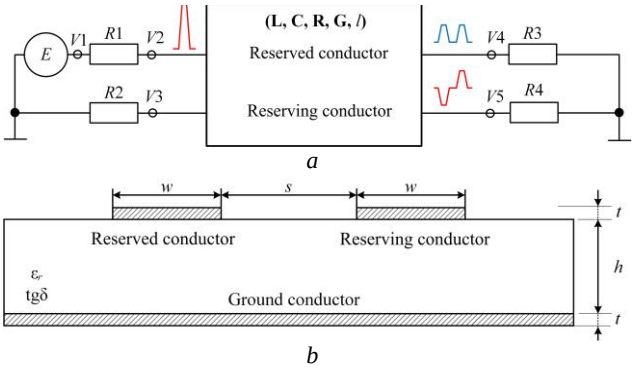

Fig. 1. Connection diagram (*a*) and cross-section (*b*) of the generalized transmission line with a single MR

is commonly used as a model for IC immunity to the effects of powerful conducted EMI. A number of studies have been conducted that investigate such a circuit solution for various purposes. For example, in [15], this model was used to analyze the effectiveness of ESD suppression. However, the efficiency of suppressing USPs of different polarities has not been evaluated. Thus, the purpose of this study is to analyze the threat of the USP of different polarities on the example of a typical IC overvoltage protection circuit.

II. Simulation Approaches and Components

The authors used schematic approaches implemented in the electronic design automation software Advanced Design System 2020 (ADS). Fig. 2 shows a connection diagram of a typical overvoltage protection system in ADS software. Fig. 3 shows unipolar and bipolar trapezoidal pulses obtained at the output of the circuits with MR (*V*4 and *V*5 nodes). The amplitude of the pulses is 1000 V, the time of the rise, fall and flat top is 100 ps, the time interval between pulses is 400 ps.

We analyzed the voltage waveforms on the *Rload* resistor (50 Ω). The analysis of an IC response to the excitation of a USP of different polarities was carried out with the activated and deactivated power supply (*SRC*2). Parasitic parameters of the diodes were considered with the series inductance *Ld* and parallel capacitor *Cd*. Parasitic parameters of supply and ground circuits were analyzed with series connected parallel *LC*-circuits. The inductance

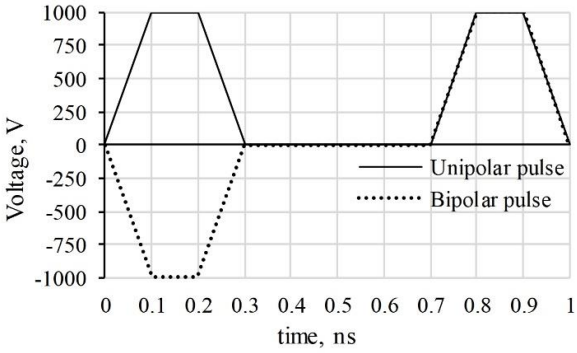

Fig. 3. Unipolar and bipolar trapezoidal pulses obtained at the output of the circuits with MR (*V*4 and *V*5 nodes)

resistance of the *LC*-circuit was 0.1 Ω. The inductance and capacitance of the *LC*-circuit were 0.1 nH and 2 pF, respectively. The common mode chokes *Lcm* and capacitors *C*4, *C*5, and the differential chokes *Ldm*1, *Ldm*2 (there is no electromagnetic coupling between the differential inductors) and capacitor *C*3 take into account the parasitic parameters of IC pins. The capacitances were 1 pF, the inductances were 0.1 nH, the coupling factor between the common mode choke inductors was 0.9.

N-norms were used to obtain the numerical characteristics of the analyzed waveforms and signals [16], [17]. Table 1 demonstrates the norms used and their characteristics [2].

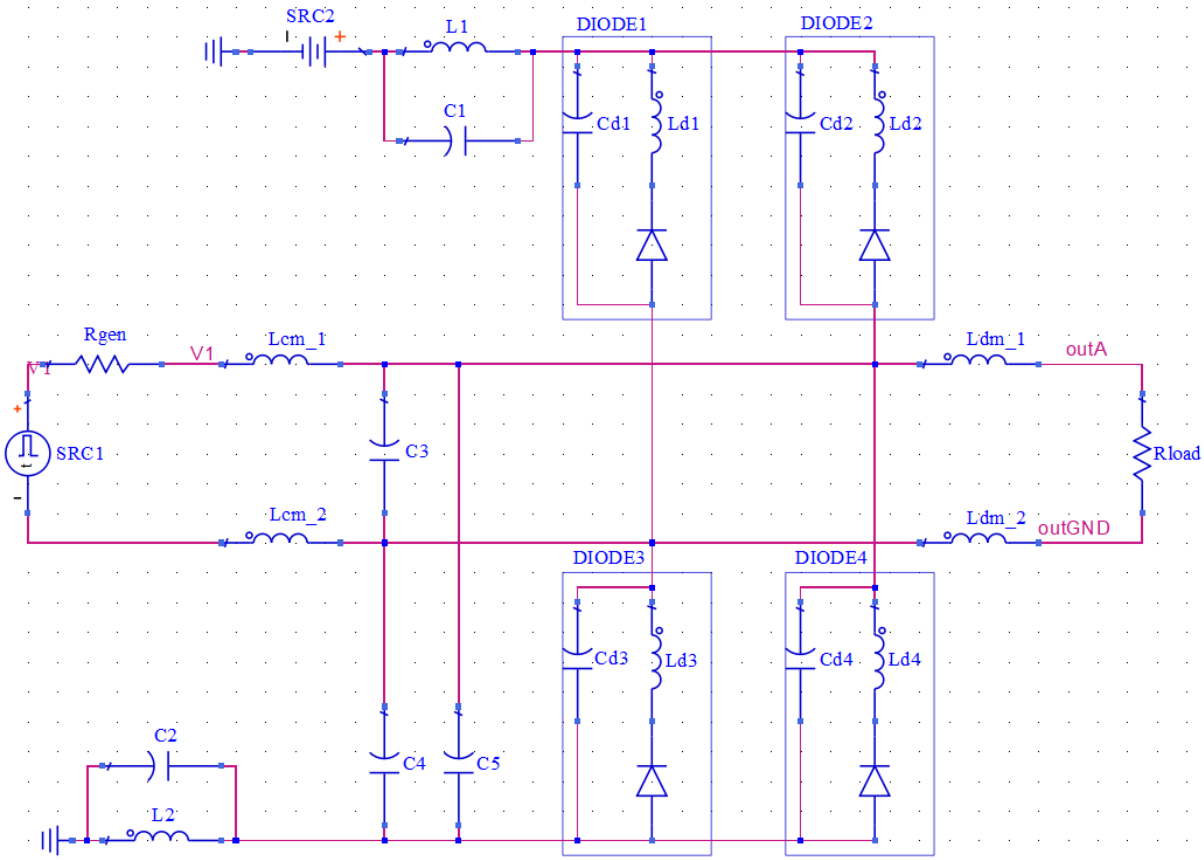

Fig. 2. Connection diagram of a typical overvoltage protection system in ADS software from [14]

III. SIMULATION RESULTS

The section presents the results of analyzing the model of IC immunity to powerful conducted emissions in circuits with a single MR. Fig. 4 shows the voltage waveforms under the influence of unipolar and bipolar pulses with and without IC power supply. The highest amplitude at the output (414 V) is observed when a USP of the same polarity is applied, and the power supply is switched off. There are two positive pulses at the output. This is caused by the fact that the diodes connected to the power supply appear to be out of service. When the circuit is exposed to USPs of different polarity, the maximum voltage is 395 V. However, there is only one positive pulse at the output. In the case when the protection circuit is connected to the power supply, the maximum voltage amplitude does not exceed 85 V. Table 2 demonstrates the *N*-norms of the waveforms under study.

The results show that there is a higher probability of component sparkling, circuit failure, dielectric breakdown, and so on in the absence of power. Thus, for example, in the case of the unipolar pulse, the value of N_2 increased by 1.69 times; in the case of the bipolar pulse, the value increased by 1.47 times. When we analyze the threat of bipolar and unipolar pulses, we can notice that in circuits with power supply the value of N_1–N_5 norms for bipolar pulses is the same or lower than for unipolar pulses. Thus, the N_1 values is 1.31 times greater, N_2 is equal, N_3 is 6.98 times greater, N_4 is 1.15 times smaller, N_5 is 1.1 times smaller. When analyzing the threat of pulses in circuits without power supply, we can see that the value of N_1–N_5 norms is also less for bipolar pulses.

Thus, it can be seen that in the case when the power is applied, the input pulses are shunted to ground or the power supply. In this case it is observed that pulses of different polarity are suppressed differently. When there is no power supply, pulses of positive polarity travel without any obstruction to the load, while pulses of negative polarity are suppressed. In this case, the shape of the pulses is strongly influenced by both matching and parasitic parameters of diodes and transmission line. It is also found that the protection system without power supplies provides better suppression of bipolar pulses than unipolar pulses. It can be assumed that the reserving conductor is in less danger than the reserved conductor.

Table 1

N-norm parameters: description and application

Formula	Name	Application
$N_1 = \lvert R(t)\rvert_{\max}$	The peak value (absolute)	Circuit failure /electric breakdown / electric arc effects
$N_2 = \left\lvert \frac{\partial R(t)}{\partial t} \right\rvert_{\max}$	The peak derivative (absolute)	Component sparkling / circuit failure
$N_3 = \left\lvert \int_0^t R(t)dt \right\rvert_{\max}$	The peak pulse (absolute)	Dielectric breakdown (if *R* means the *E* field)
$N_4 = \int_0^\infty \lvert R(t)\rvert dt$	Rectified general pulse	Equipment damage
$N_5 = \left\{ \int_0^\infty \lvert R(t)\rvert^2 dt \right\}^{\frac{1}{2}}$	The square root of the action integral	Component burnout

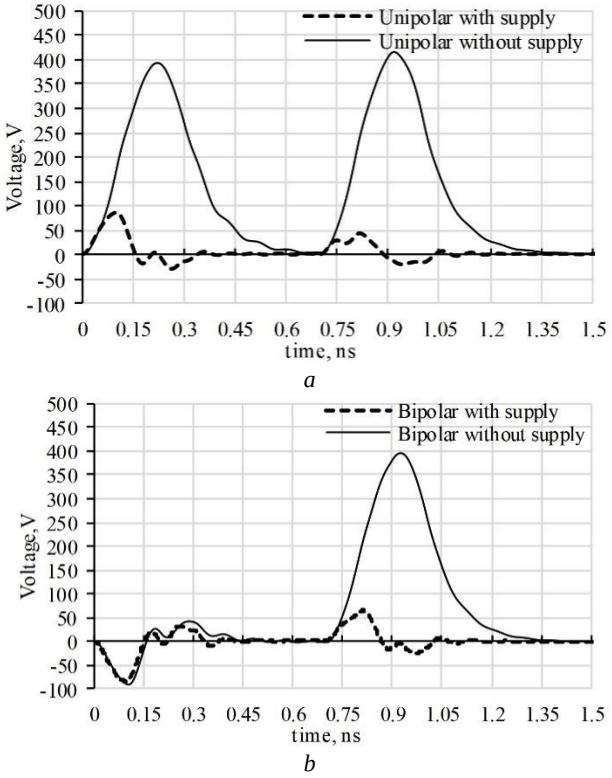

Fig. 4. Voltage waveforms under the influence of unipolar (*a*) and bipolar (*b*) pulses with and without power supply

Table 2

N-norm of the waveforms under study

	Unipolar with supply	Unipolar without supply	Bipolar with supply	Bipolar without supply
N_1	85.68	414.2	65.31	395.46
N_2	$2.03 \cdot 10^{12}$	$3.44 \cdot 10^{12}$	$2.01 \cdot 10^{12}$	$2.96 \cdot 10^{12}$
N_3	$0.817 \cdot 10^{-8}$	$19.5 \cdot 10^{-8}$	$0.117 \cdot 10^{-8}$	$9.503 \cdot 10^{-8}$
N_4	$0.179 \cdot 10^{-7}$	$1.941 \cdot 10^{-7}$	$0.206 \cdot 10^{-7}$	$1.104 \cdot 10^{-7}$
N_5	$0.842 \cdot 10^{-3}$	$7.44 \cdot 10^{-3}$	$0.928 \cdot 10^{-3}$	$5.221 \cdot 10^{-3}$

IV. Conclusion

During the operation of REE, there are complex transients that can generate conducted USPs. They can damage REE and bypass traditional interference protection devices due to their limited performance. Modal Reservation (MR, or modal redundancy) is used to improve the reliability, fault tolerance, and noise immunity of the REE. When passing the USP on the MR circuit, two unipolar pulses are generated at the far end of the reserved (or primary) conductor, and two bipolar pulses are generated at the far end of the reserving (or secondary) conductor. Thus, with a large sufficient amplitude and short duration of the USP, the components of the transmission line may be at risk. To protect high-speed ICs against overvoltages and conducted emissions, dual diodes are most commonly used. In this paper, the authors presented the results of the analysis of the model of IC immunity to powerful conducted emissions in circuits with a single MR. The results show in circuits with MR the probability of failure of the reserved circuit is lower than that of the reserving circuit. This is partially caused by the fact that the negative part of the bipolar pulse is shunted to the ground through diodes. At the same time, in circuits without power supply, the positive components of both unipolar and bipolar pulses are able to unobstructedly penetrate and damage equipment. The parasitic parameters of diodes can significantly limit the speed of operation. Concurrently, the combined use of the dual diode system with passive protection devices based on modal filtration (with a high level of interference suppression) allows achieving a desirable level of conducted interference attenuation even in the presence of unwanted parasitic parameters. The perspective of this study is to conduct an experimental study to confirm the results of the circuit simulation. It is also relevant to study the effectiveness of such protection against other types of pulses.

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Моделирование устойчивости интегральных схем к мощным кондуктивным воздействиям в цепях с однократным модальным резервированием

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***Аннотация*—Статья представляет результаты анализа модели устойчивости интегральных схем к мощным кондуктивным воздействиям в цепях с однократным модальным резервированием. Используются однополярные и разнополярные импульсные воздействия на интегральную схему с поданным питанием и без него. Результаты показали, что защита от перенапряжения на основе сдвоенных диодов без источника питания лучше защищает от биполярных импульсов. Эффективность такой защиты сильно зависит от паразитных параметров. При этом при увеличении верхней граничной частоты нежелательных воздействий эта эффективность может снизиться. В то же время совместное применение диодной и пассивной защиты на основе модальной фильтрации способно обеспечить желаемый уровень ослабления кондуктивных помех даже при наличии паразитных параметров.**

***Ключевые слова*— интегральные схемы, сверхкороткий импульс, электромагнитная совместимость, модальное резервирование, схемотехническое моделирование.**

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