

Optimization of Stack Parameters of Multi-layer PCB for Circuits with Redundancy by Genetic Algorithm

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Abstract— The increase of noise immunity of circuits with redundancy is considered. A new method for packaging and tracing of printed circuit boards (PCBs) with redundancy is described. The method is characterized by increased noise immunity due to modal filtration. Optimization of stack parameters of a multi-layer PCB for the implementation of the new method is performed by the genetic algorithm. For the formulation of an objective function, the calculated elements of characteristic impedance matrix of coupled transmission lines are used. The obtained optimal parameters allow matching the reserved and reserving lines with a load of 50 Ω . The Optimization permitted to develop the PCB prototype with different samples of coupled transmission lines. The photo of the manufactured prototype is given.

Keywords— *Modal filtration, redundancy, noise immunity, optimization, genetic algorithms*

I. INTRODUCTION

Implementation of science and technology achievements, modern technology is characterized by the creation of complex systems with a high level of automation devices that perform an intelligent and adaptive control functions in space and aviation technology, thermal and nuclear power generation, chemical, petrochemical, oil and gas, metallurgical processing and other industries and transport systems. Successful solution of management tasks related to increasing the efficiency of production put as a priority the problem of ensuring the high reliability of such systems and technical means. The importance of this problem is due to the possible significant damage that can occur in hazardous industries and industries with large capacities [1].

Redundancy is practically the only and widely used method for improving the reliability of automation systems. It allows the creation of alarm systems, emergency protection, automatic fire extinguishing, monitoring and management of explosive technological blocks [2] and other systems related to safety levels SIL1-SIL3 in accordance with IEC 61508-5 [3], as well as responsible systems in which even a short down time leads to large financial losses (electricity distribution systems, management of continuous technological processes, tracking of moving objects, etc.). Redundancy allows the creation of highly reliable systems from typical wide-range products [4] using a similar, inactive part of electronic equipment in the case of a damage in the functioning part.

In addition, a threat of intentional electromagnetic interference impact on electronic equipment is growing [5]. Such the impact can lead to malfunction of electronic equipment [6]. Particularly, the impact of ultrashort pulses (USP) is especially dangerous, as existing surge protectors do not protect against them [7]. There are only some industrial devices that protect against USP but they have large dimensions and high cost. Thus, currently, there is no both low-cost and effective protection against UWB pulses. However, the increasing role of electronics makes this protection more urgent. The need for proper protection against USP significantly complicates all parts and, as a consequence, the final design of the systems. Meanwhile, the presence of redundancy allows looking for ways to use it rationally.

Based on accounting the electromagnetic coupling between reserved and reserving conductors of the reserved and reserving circuits, a method of modal reservation [8, 9] can improve the protection of electronic systems against electromagnetic interference. In the paper [10] the possibility of modal redundancy realization in various types of interconnects, including multi-layer PCBs is shown. However, in practice, it is rather difficult to produce the multi-layer PCB with geometric parameters obtained in this paper. In particular, in order to implement the modal reservation mock-up, it is necessary to optimize the stack of the mock-up for the parameters of a typical process for PCB manufacturing.

The aim of this paper is to optimize the stack of the breadboard construction that implements modal reservation, taking into account the technical processes of PCB manufacturing. For this, the genetic optimization algorithm is first briefly described. Then, optimization of the parameters and modelling of the characteristics based on the optimization results were carried out. Finally, the ML PCB stack and the mock-up are presented.

II. GENETIC ALGORITHM OPTIMIZATION OF THE MOCK-UP

The genetic algorithm (GA) is an evolutionary algorithm, the main idea of which is combining (crossing). The algorithm is divided into three main stages: crossing (formation of the population), selection (selection) and formation of a new generation. Steps are repeated until the result is acceptable or the number of generations (cycles) reaches the specified value. In general, the use of GA makes it possible to eliminate the

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problem of an exhaustive search. Therefore, GA is widely used in solving a variety of tasks.

In this paper, the GA parameters were chosen as follows: number of individuals – 30, number of generations – 30, mutation factor – 0.5, crossover coefficient – 0.5. During optimization, the deviation of the geometric mean value of the impedances of the even and odd modes from 50 Ω, calculated from the entries of the characteristic impedance matrix **Z** as $Z_o=Z_{11}-Z_{21}$, $Z_e=Z_{11}+Z_{21}$, was minimized. The boundary conditions for calculating the time response were chosen from condition

$$R=(Z_o Z_e)^{0.5} \tag{1}$$

The cross-section and the schematic diagram are shown in Fig. 1. The calculations were carried out in the TALGAT system [11].

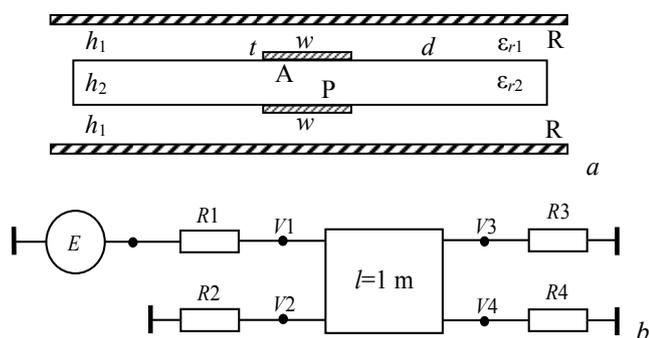


Fig. 1. The cross-section of multi-layer PCB (a) and schematic diagram (b)

Without taking into account the real parameters (Table I), which are used for PCB manufacturing, it is possible to obtain an attenuation of a pulse by factor 5 (Fig. 2) and diagonal values of the matrix equal to 50 Ω. However, in this case, the geometric mean value of the impedances of the even and odd modes is relatively small and does not reach 50 Ω. The dependences of the value on the electrophysical and geometric parameters are shown in Figs. 3–6.

TABLE I. PARAMETERS OF MODAL RESERVATION MOCK-UP CROSS-SECTION WITHOUT ACCOUNTING THE REAL VALUES

| Parameters | | | | | | | Z, Ω | |
|------------|-------|--------|--------|-----|-----|----------|------|----|
| w, μm | t, μm | h2, μm | h1, μm | εr1 | εr2 | Δτ, ns/m | 50 | 49 |
| 300 | 65 | 10 | 630 | 5 | 25 | 8,7 | 49 | 50 |

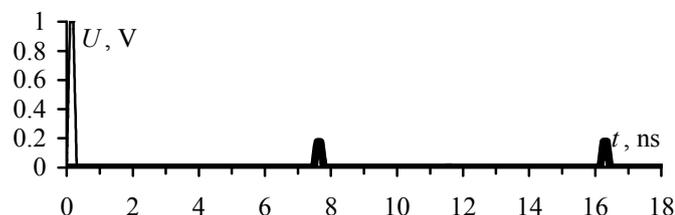


Fig. 2. Waveforms at near (→) and far (←) ends of active line

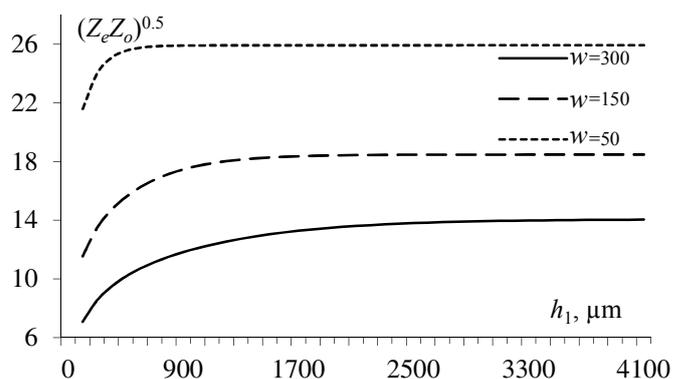


Fig. 3. Dependences of $(Z_e Z_o)^{0.5}$ on h_1 for different w , μm

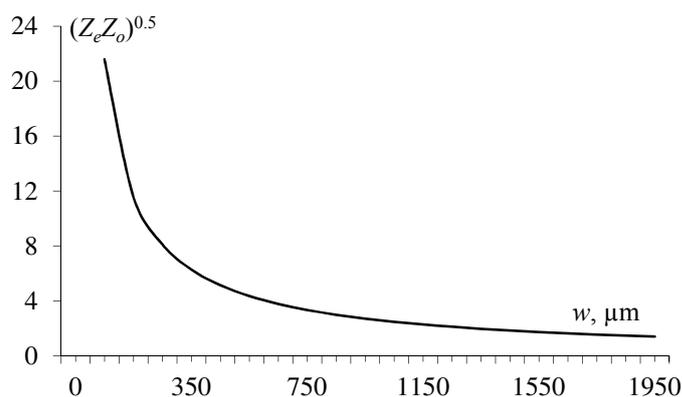


Fig. 4. Dependence of $(Z_e Z_o)^{0.5}$ on w

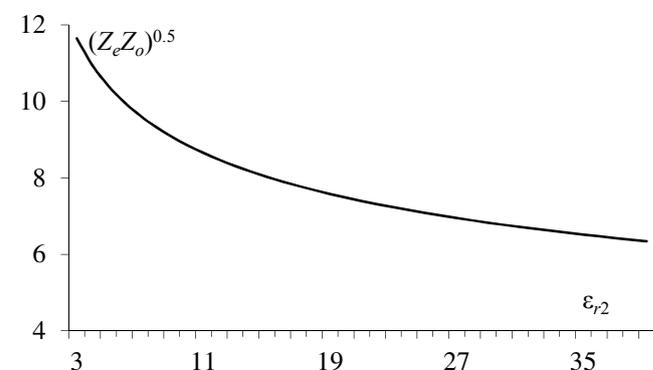


Fig. 5. Dependence of $(Z_e Z_o)^{0.5}$ on ϵ_{r2}

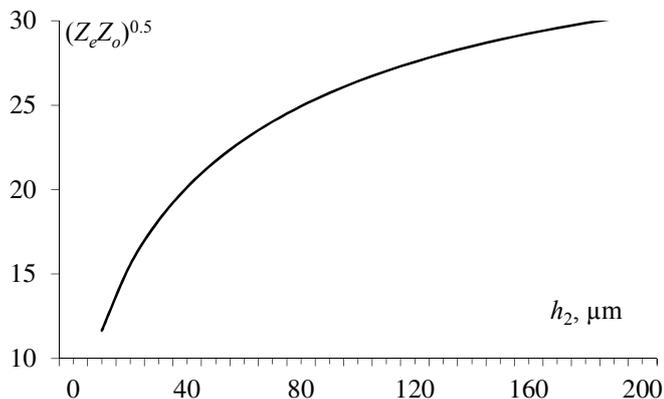


Fig. 6. Dependence of $(Z_e Z_o)^{0.5}$ on h_2

The modern nomenclature of radioelectronic materials and the possibilities of technological processes for manufacturing printed circuit boards limit the spectrum of geometric and electrophysical parameters. When developing the stack of mock-up, the Rogers RO3010 was chosen as a dielectric because of the low layer thickness (130 μm) and the high value of ϵ_r . The FR 4 1080 was chosen as a prepreg. The parameters of a typical manufacturing process for multi-layer PCB and the results of optimization, with their consideration, are summarized in Table 2 and 3 respectively. The calculated matrices of the primary parameters are summarized in Table 4. The response to the impulse excitation and the dependence of the geometric mean value of the impedances of the even and odd modes are shown in Fig. 7, 8 respectively.

TABLE II. THE PARAMETERS OF A TYPICAL MANUFACTURING PROCESS FOR MULTI-LAYER PCB

| $w, \mu\text{m}$ | $t, \mu\text{m}$ | $H_2, \mu\text{m}$ | $h_1, \mu\text{m}$ |
|------------------|------------------|--------------------|--------------------|
| ≥ 130 | 5...105 | ≥ 130 | ≥ 68 |

TABLE III. PARAMETERS OF CROSS-SECTION OF MODAL RESERVATION MOCK-UP WITH ACCOUNTING TECHNOLOGICAL PROCESSES FOR PCB MANUFACTURING

| Parameters | | | | | | | $(Z_e Z_o)^{0.5}, \Omega$ |
|------------------|------------------|--------------------|--------------------|-----------------|-----------------|---------------------------|---------------------------|
| $w, \mu\text{m}$ | $t, \mu\text{m}$ | $h_2, \mu\text{m}$ | $h_1, \mu\text{m}$ | ϵ_{r1} | ϵ_{r2} | $\Delta\tau, \text{ns/m}$ | 50 |
| 185 | 35 | 130 | 600 | 4.25 | 10.2 | 2.19 | |

TABLE IV. THE MATRICES OF THE PRIMARY PARAMETERS OF THE STRUCTURE

| $L, \text{nH/m}$ | | $C, \text{pF/m}$ | | Z, Ω | |
|------------------|-------|------------------|--------|-------------|----|
| 524,7 | 310,9 | 243,4 | -179,5 | 68 | 46 |
| 310,9 | 524,7 | -179,5 | 243,4 | 46 | 68 |

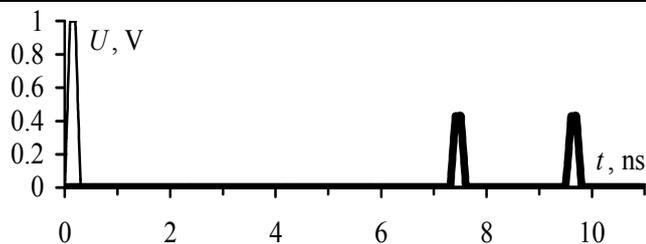


Fig. 7. Waveforms at near (—) and far (—) ends of active line of the optimized multilayer PCB

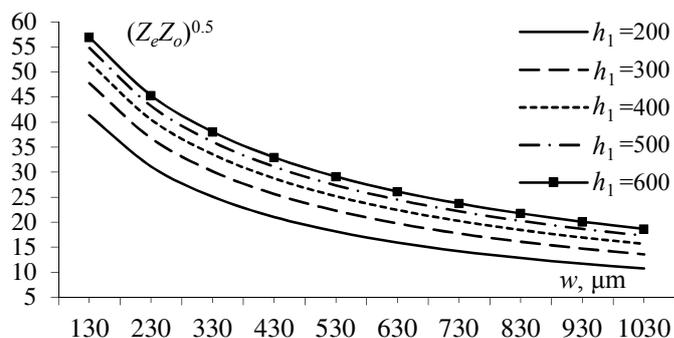


Fig. 8. Dependences of $(Z_e Z_o)^{0.5}$ on w for different $h_1, \mu\text{m}$

Figure 9 shows the time response to the actual pulse excitation, taking into account the parameters of the stack of multilayer PCB obtained during optimization, and the loads at the ends of the lines equal to 50 Ω (line length is 40 cm). The equality of the amplitudes of the decomposed pulses indicates the proper matching.

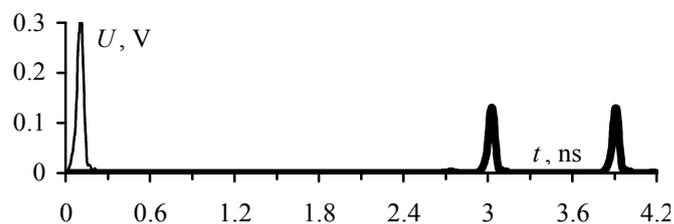


Fig. 9. Waveforms at near (—) and far (—) ends of active line with length of 40 cm for the optimized ML PCB

Structural diagram of the stack with the parameters obtained after optimization is shown in Fig. 10. The photograph of the manufactured mock-up is shown in Fig. 11. The mock-up includes sets (by the number and length of lines) of electrical connections designed to take into account the modal reservation method being developed. In addition to the original reservation option for a single line, an option is implemented for reserving the two lines with a strong edge coupling, which allows assessing the effect of the tracing density on modal distortions and the conditions of line matching. The mock-up includes footprints for SMA connectors at the ends of reserving and reserved electrical connections. This solution allows to carry out measurements in any interesting line, and also to set the boundary conditions at their ends.

| Material | Thickness |
|-------------------|-----------|
| Copper foil | 0.035 mm |
| Prepreg FR-4 1080 | 0.6 mm |
| Copper foil | 0.035 mm |
| Rogers RO3010 | 0.13 mm |
| Copper foil | 0.035 mm |
| Prepreg FR-4 1080 | 0.6 mm |
| Copper foil | 0.035 mm |

Fig. 10. The structure of multi-layer PCB layers (thickness of PCB of 1.47 mm)

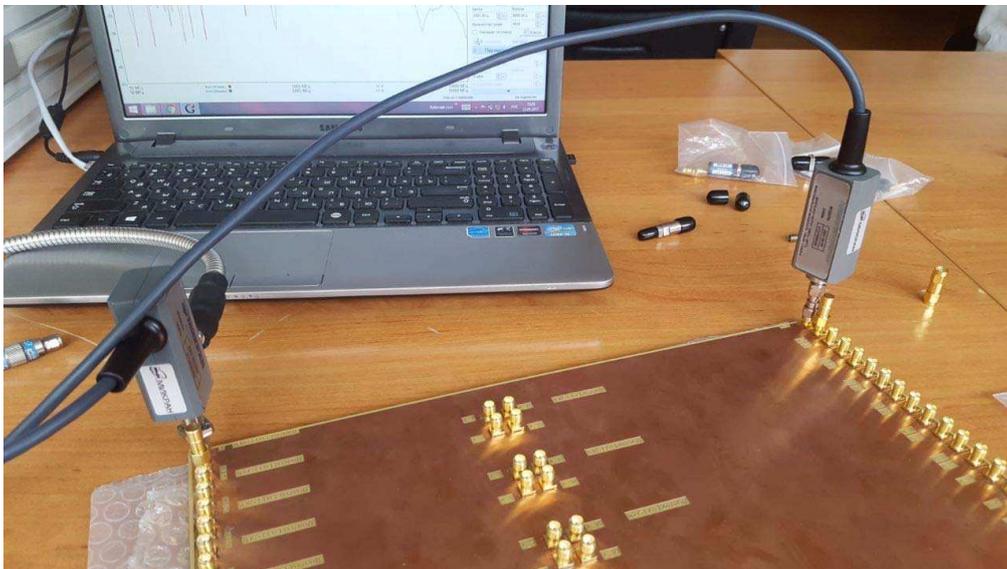


Fig. 11. Photograph of the manufactured mock-up with the scalar network analyser P2M-40 connected to it

III. CONCLUSION

Thus, the optimization of the stack of mock-up, realizing the modal reserving taking into account the typical manufacturing process of multi-layer PCB, was performed. The influence of the coupling between the conductors on the attenuation of the impulse noise and the geometric mean value of the impedances of the even and odd modes (and, accordingly, on the match of the line as a whole) is shown. Geometric parameters are obtained, on the basis of which the final stack of the mock-up is constructed.

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